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# MS-7817

mATX  
Ver: 12

## Intel Sharkbay plamform H81

**CPU:** INTEL-Haswell LGA1150

**System Chipset:** INTEL-LYNX

**Memory:** DDRIII (1333/1666MHz) \* 2 (Dual Channel)

**PWM:** VRD12 - ISL95812

**OnBoard Chipset:**

HD Audio Codec:RTL892

LAN-realtek8111G

SIO:NUVOTON 5533D

SPI ROM: 64 MB

**Other:**

DVI\*1

VGA\*1

SATA2\*2

SATA3\*2

FRONT USB2.0 \*2

REAL USB2.0 \*4

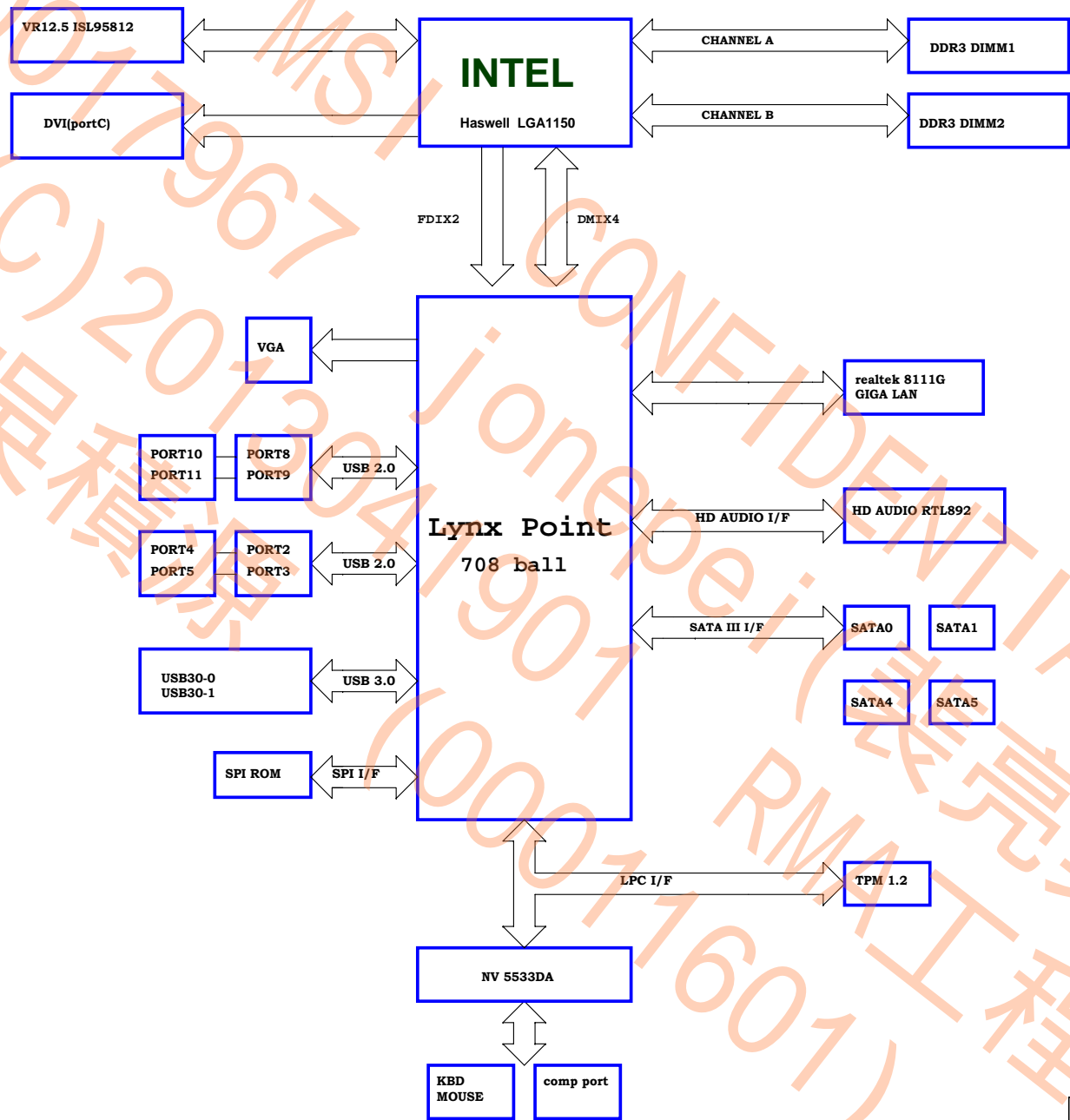
REAL USB3.0 \*2

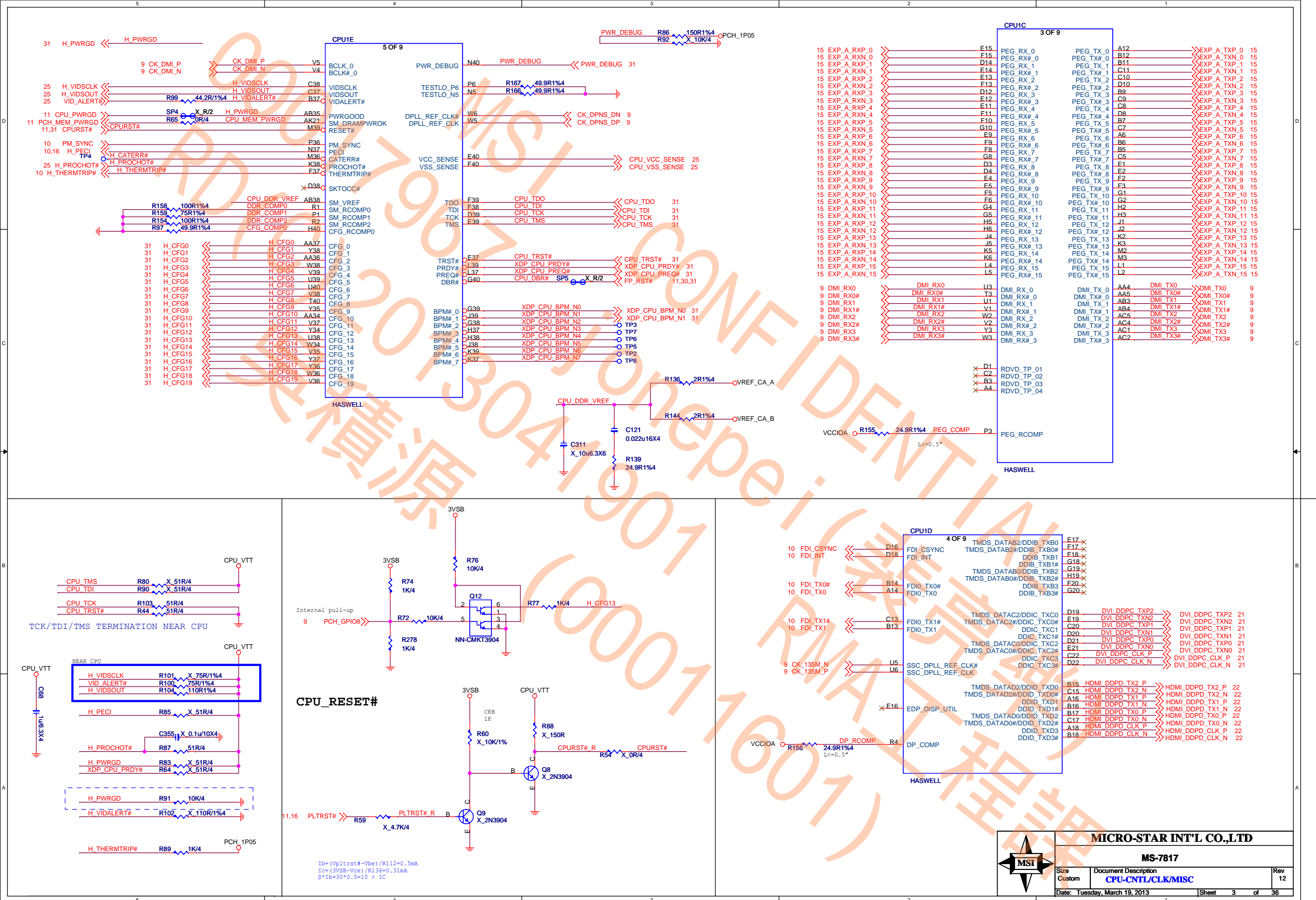
**Expansion Slots:**

PCI Express (X16) Slot \* 1

PCI Express (X1) Slot \* 1

MS-7817 Block Diagram











GND

GND



MICRO-STAR INT'L CO.,LTD

MS-7817

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4 MEM\_MA\_DATA[63..0]

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MEM\_MA\_DATA63

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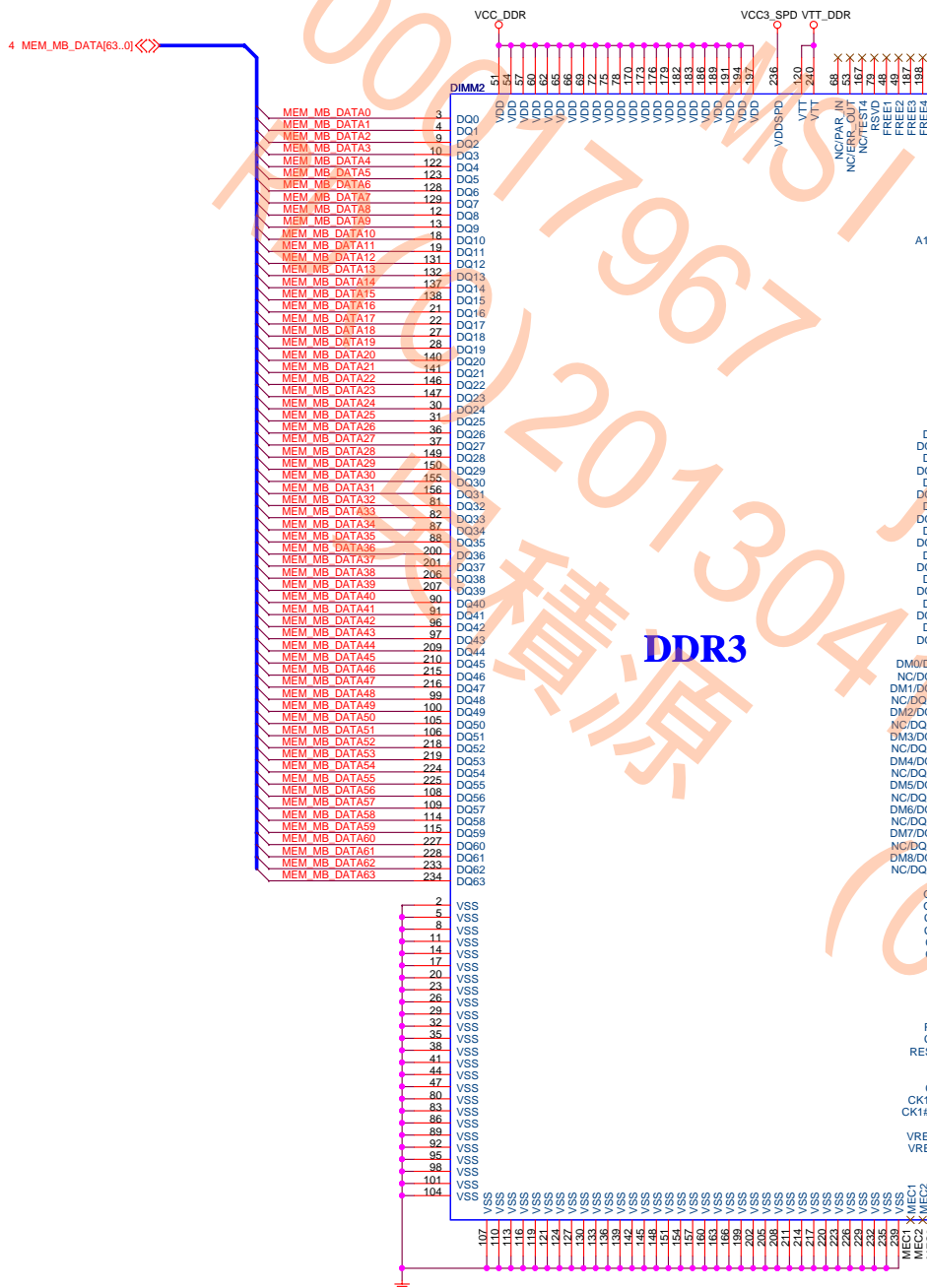
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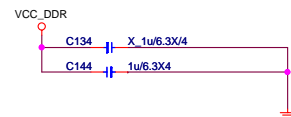
# DDR3 DIMM\_B0



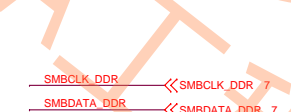
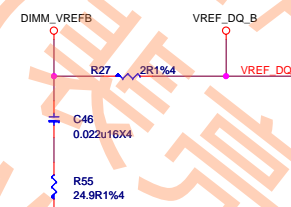
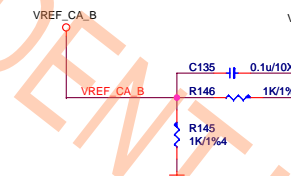
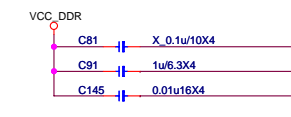
DDR3

DDEII-240\_BLUE-R

Place close to DIMM2

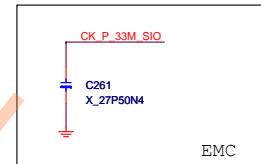


Place close to DIMM2



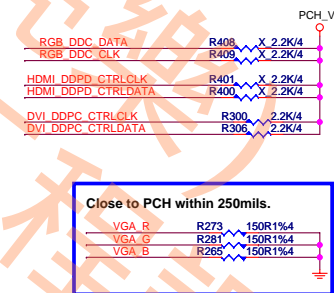
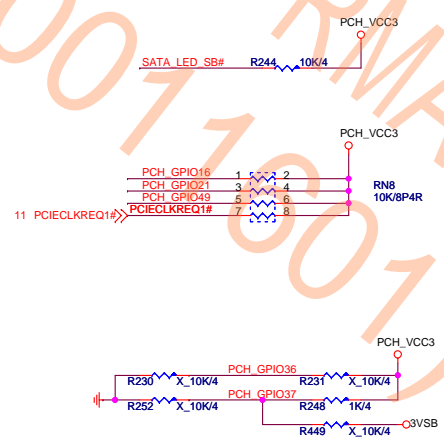
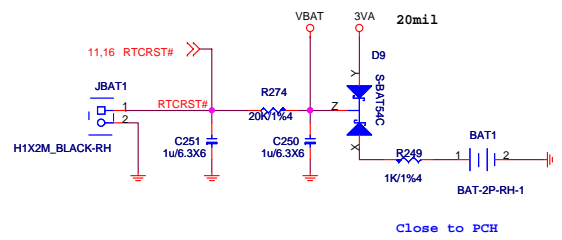
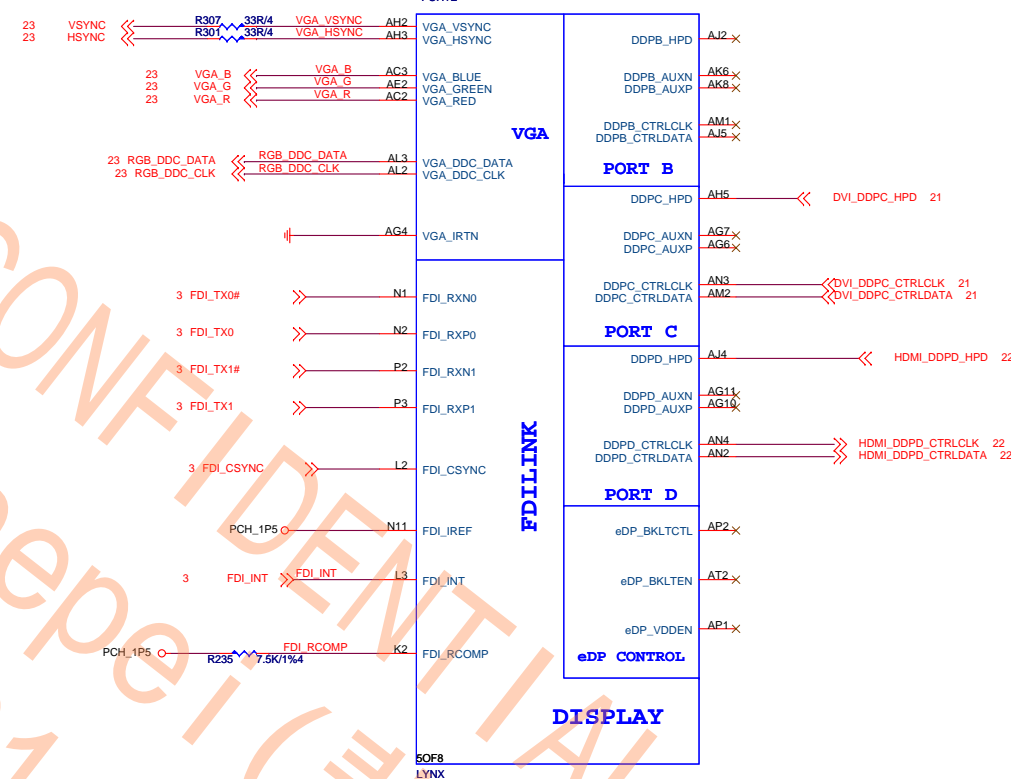


```
pcie port7,8 NA
```



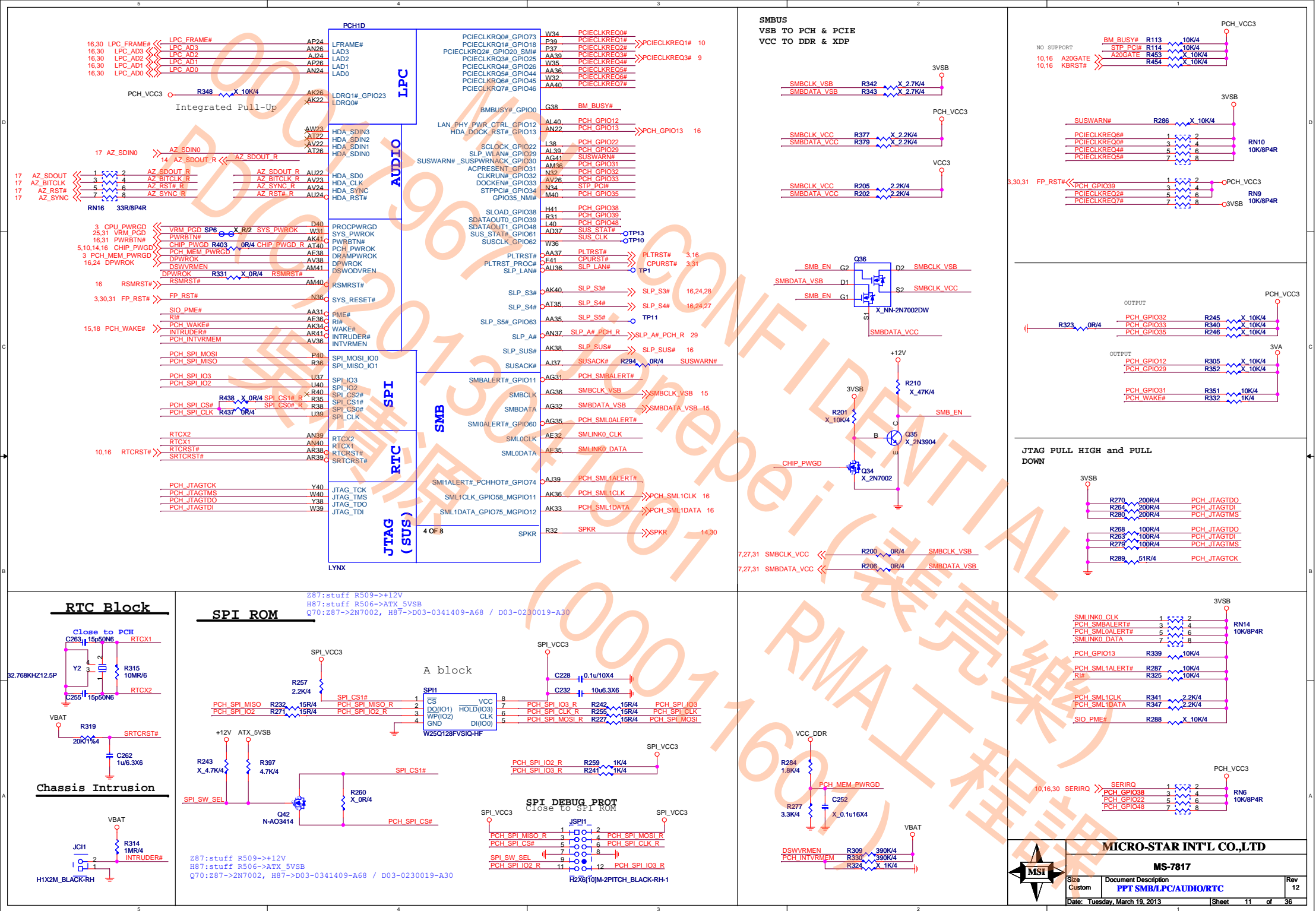
Size Custom	Document Description <b>PPT PCIE/DMI/USB/CLK</b>	Rev 12
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SATA 6 Gb/s support on ports 0 and 1 only.

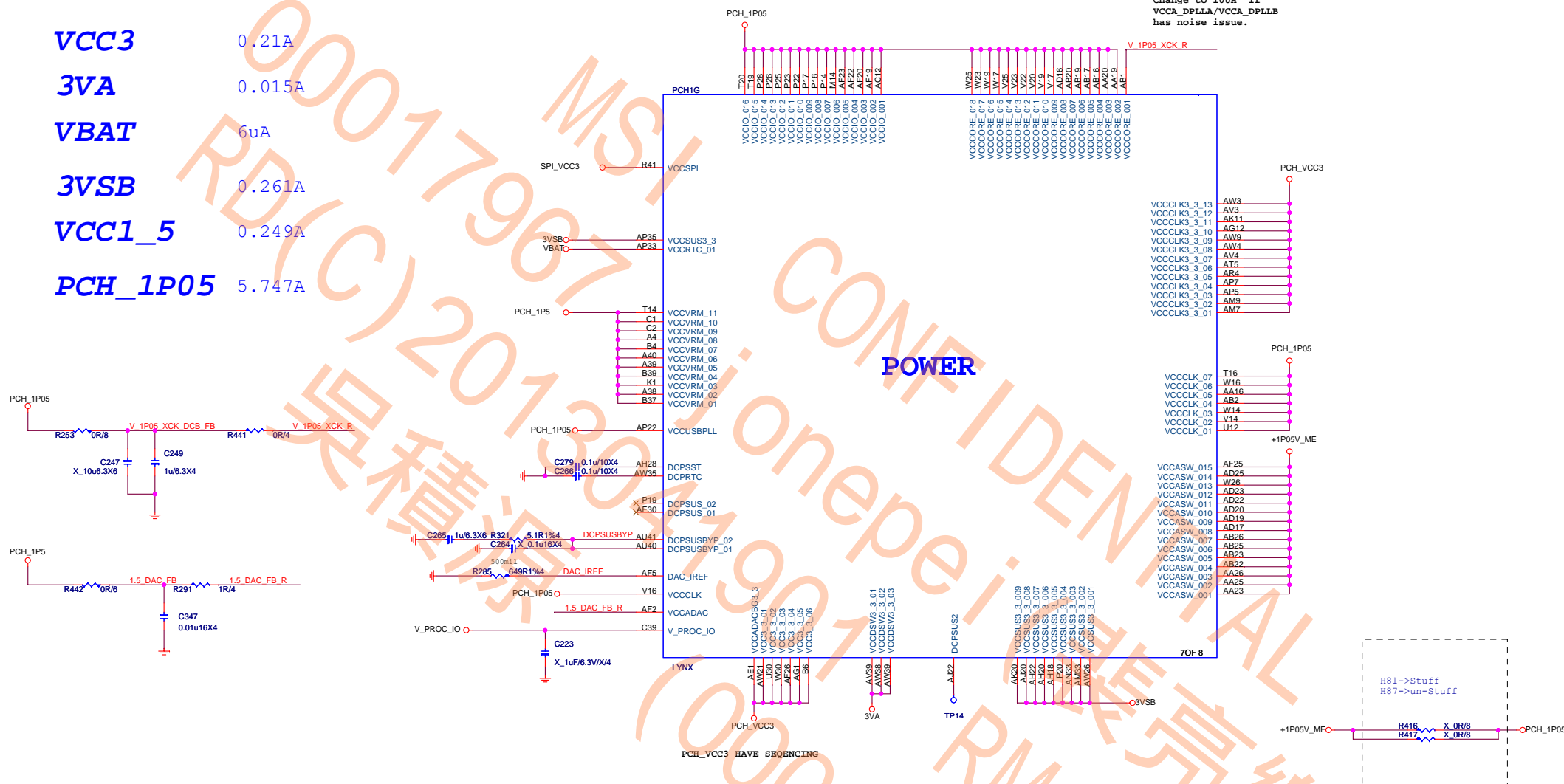


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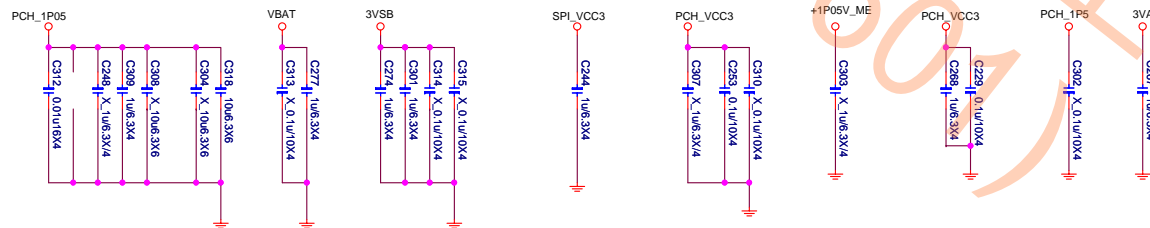
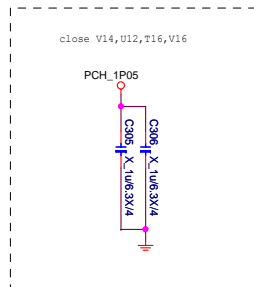
Size Custom	Document Description <b>PPT SATA/HOST/FAN/GPIO/VGA</b>	Rev 12
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<b>VCC3</b>	0.21A
<b>3VA</b>	0.015A
<b>VBAT</b>	6uA
<b>3VSB</b>	0.261A
<b>VCC1_5</b>	0.249A
<b>PCH_1P05</b>	5.747A



PCH decoupling cap



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00017901  
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MSI  
CONFIDENTIAL  
RMA (售后服务)  
1601



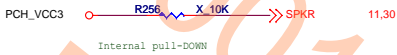
MICRO-STAR INT'L CO.,LTD

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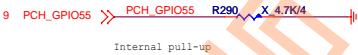


PCH Straps



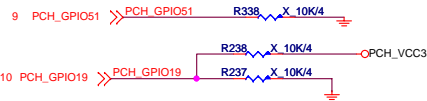
**SPKR**

**Default Mode:**  
Internal weak Pull-down.  
**No Reboot Mode with TCO Disabled:**  
Connect to Vcc3\_3 with 8.2k~10k Ohm weak pullup resistor.



**GPIO55**

**Default Mode:**  
Internal pull-up.  
**Top Block Swap Mode:**  
Connect to ground with 4.7k Ohm weak pulldown resistor.



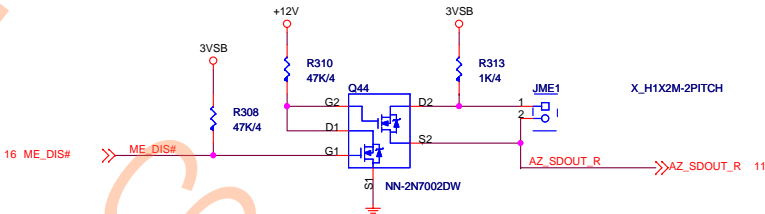
**SATA1GF/GPIO19, GPIO51**

**Default (SPI):**  
Left both SATA1GF/GPIO19 and GPIO51 floating.  
No pull up required.  
**Boot from PCI:**  
Connect SATA1GF/GPIO19 to ground with 1k Ohm pull-down resistor.  
Leave GPIO51 Floating.  
**Boot from LPC:**  
Connect both SATA1GF/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.



**GPIO53**

Do not pull low.  
Connect to ground with 1k Ohm pull-down resistor.



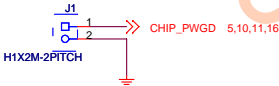
**HDA\_SDO**

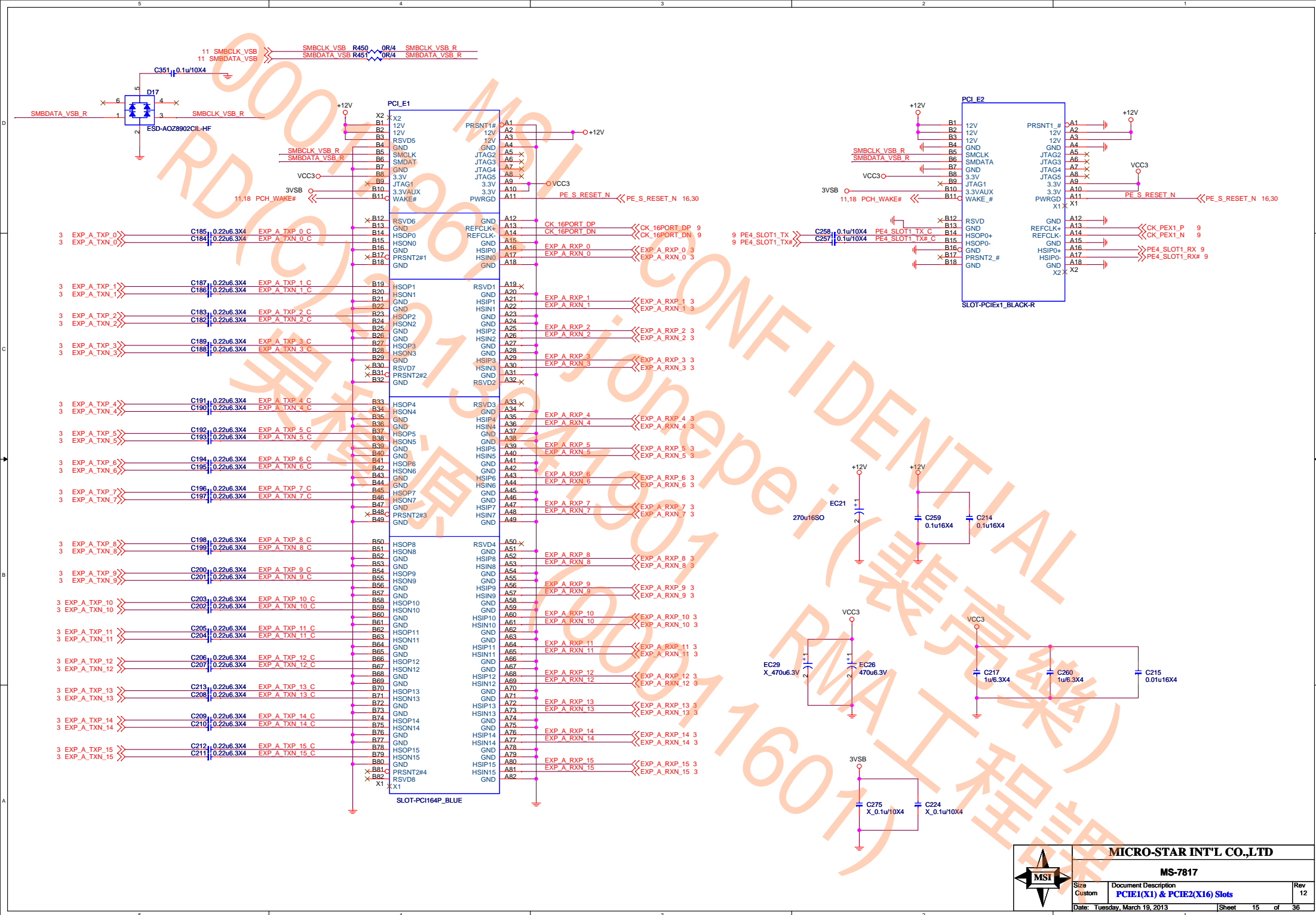
**Default:**  
Do not pull high.  
**Disable ME in Manufacturing Mode:**  
Connect to VccSusHDA with 1k Ohm pull-up resistor through a jumper.

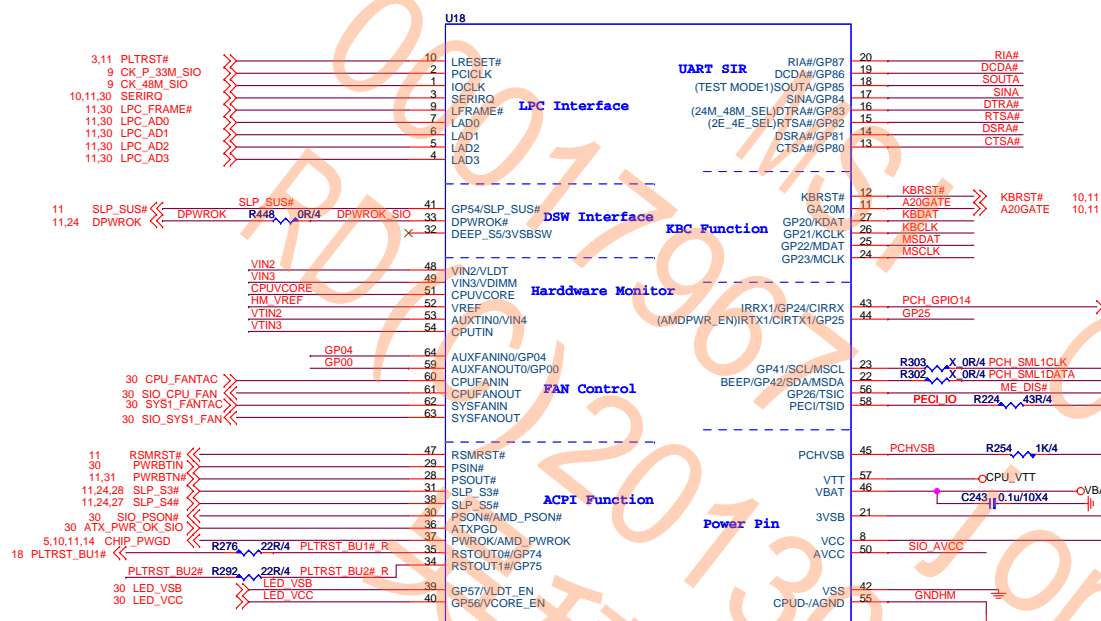
**GPIO37**

**Enable TLS:**  
Pull up with 1k Ohm to VccSus3.3.  
**Default (Disable TLS):**  
Leave NC. Internal pull down.

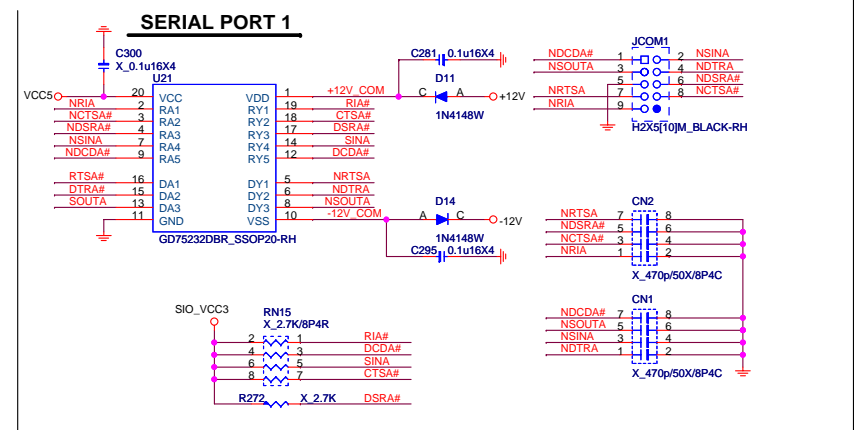
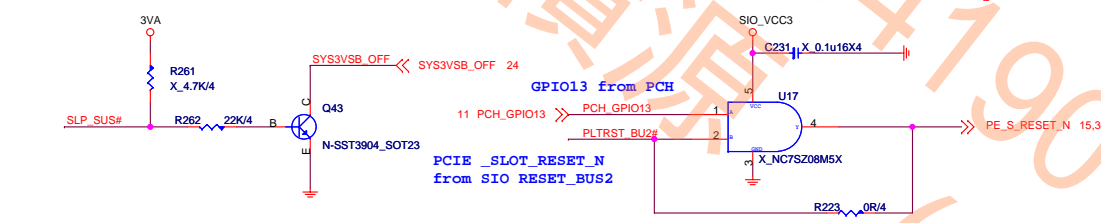
For test cpu voltage



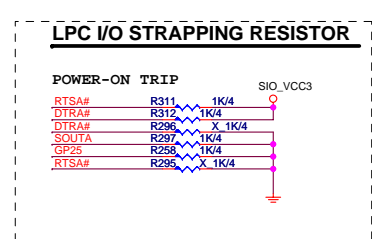
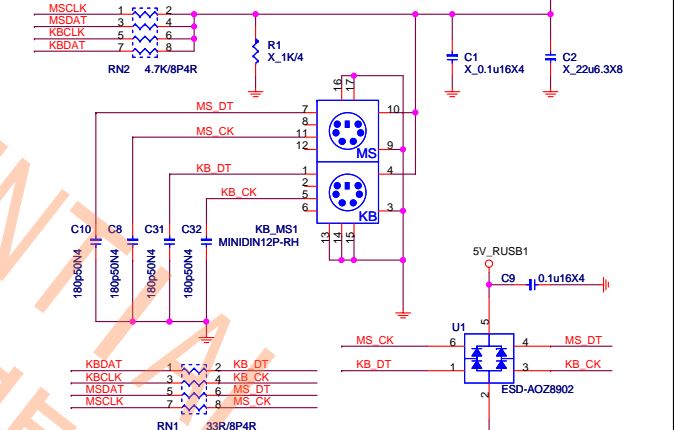




### 5533D DSW SUPPORT



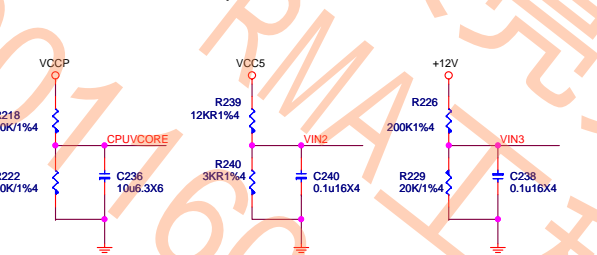
### PS2 Connector



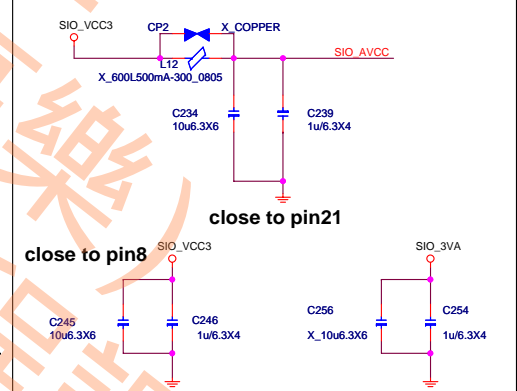
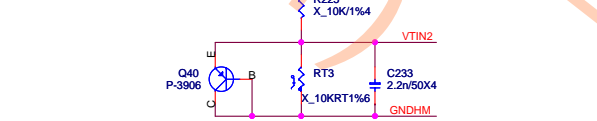
### NCT5533D POWER ON STRAPPING PIN

PIN	Function	NET Name	HI	LO
44	AMD_PWR_EN		ENABLE AMD PWR SEQ	DISABLE AMD PWR SEQ
18	TEST_MODEL	SOUTA	TEST MODE 1 ENABLE	TEST MODE 1 DISABLE
16	24M_48M_SEL	DTRA#	48MHz	24MHz
15	2E_4E_SEL	RTSA#	4E	2E

### Voltage Sensing



### Thermal Resistor



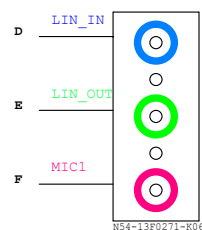
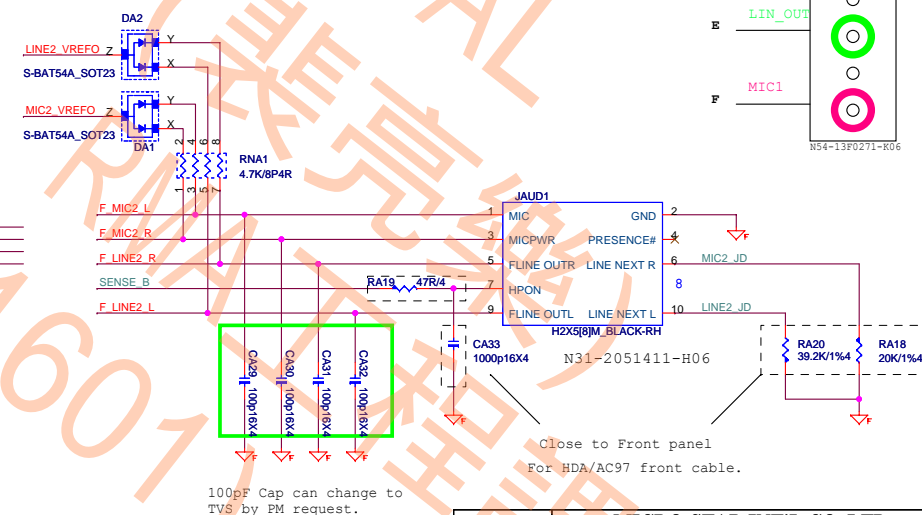
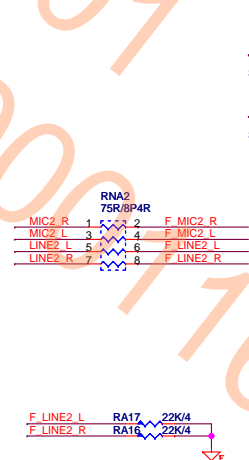
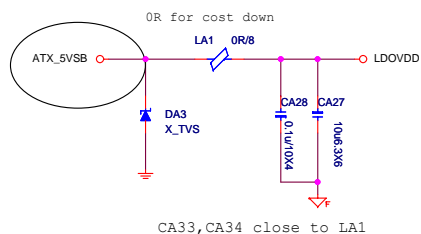
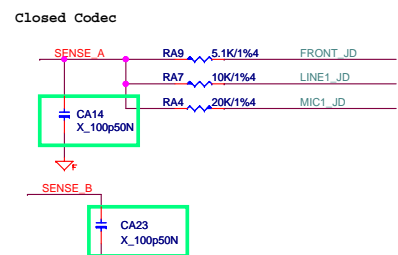
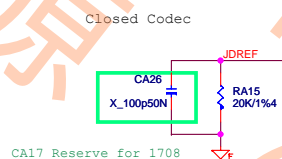
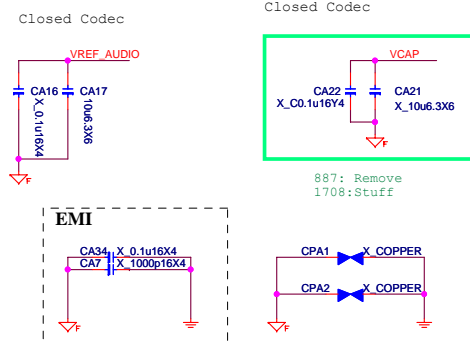
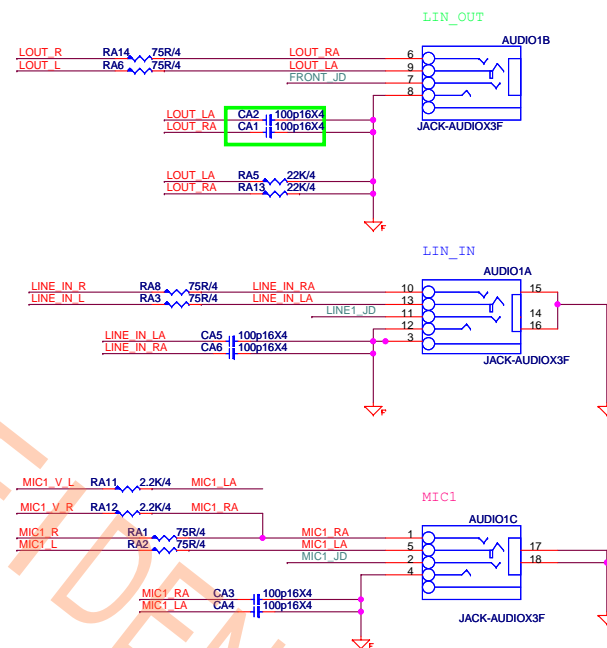
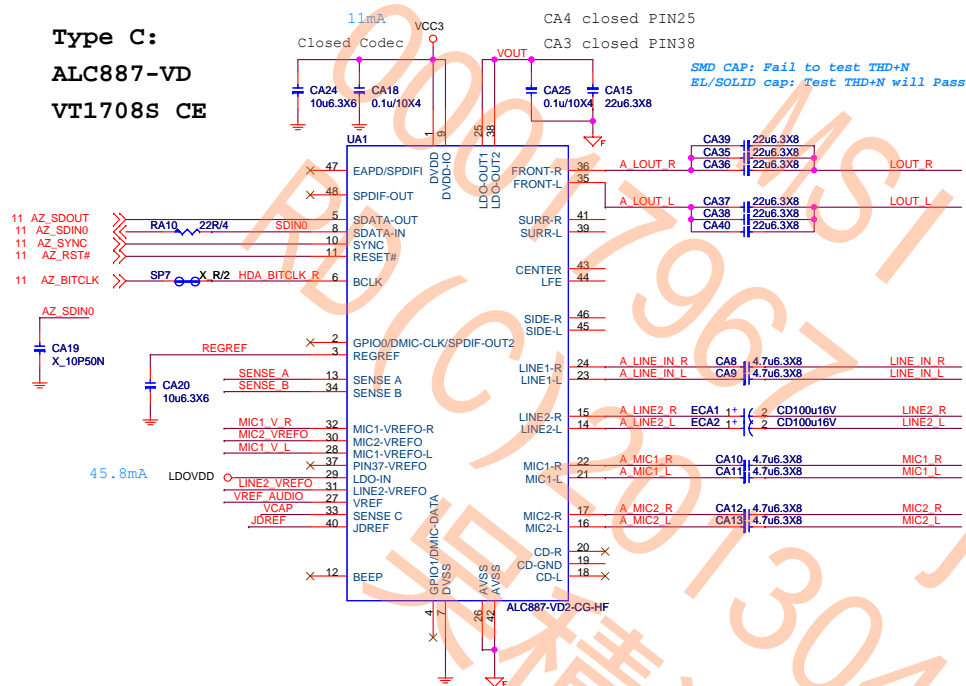
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**MS-7817**

Size: Custom Document Description: SIO-NUVOTON NCT5533D Rev: 12

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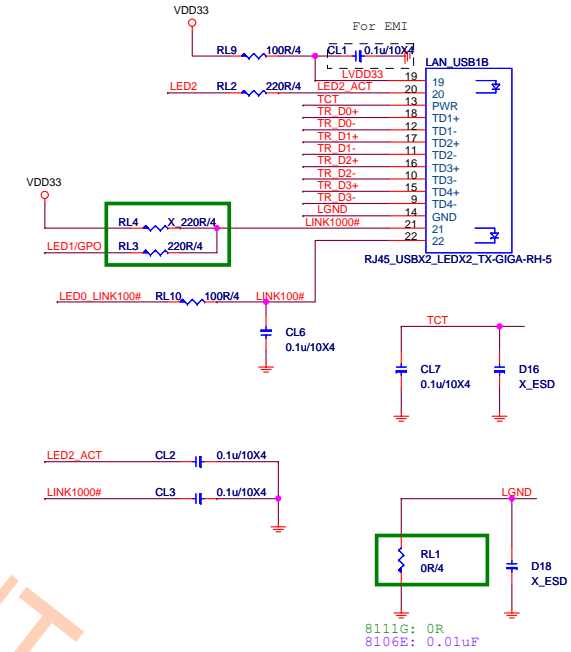
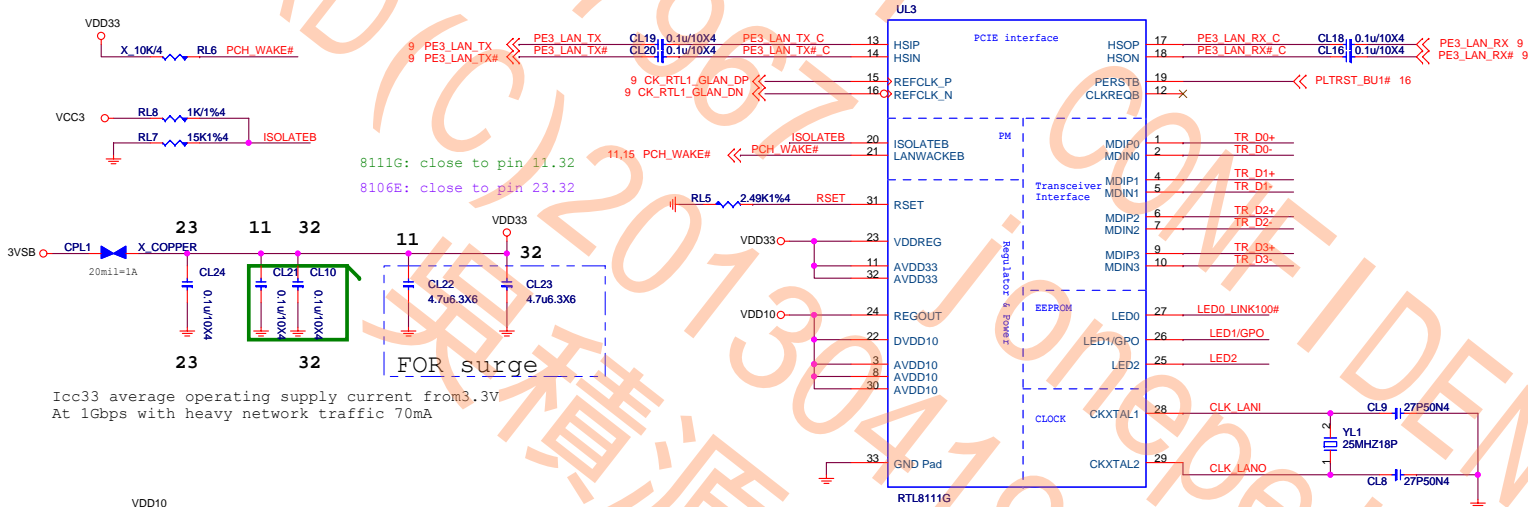
Type C:  
ALC887-VD  
VT1708S CE



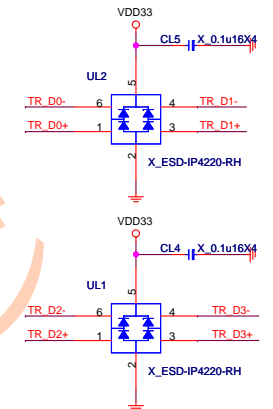
# RTL8111G Giga LAN

## RTL8106E 10/100M LAN

### LAN Connector



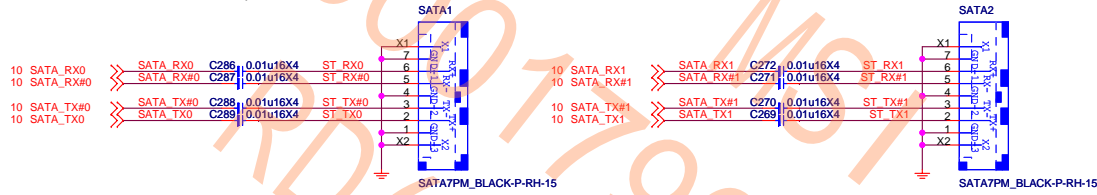
### Reserve ESD Protect



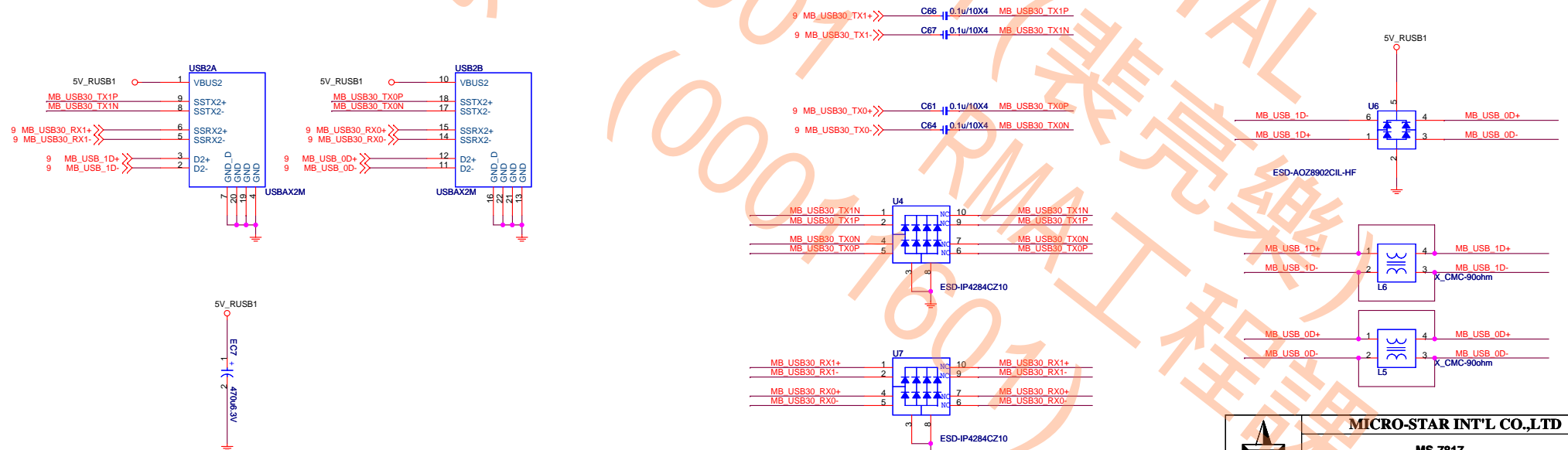
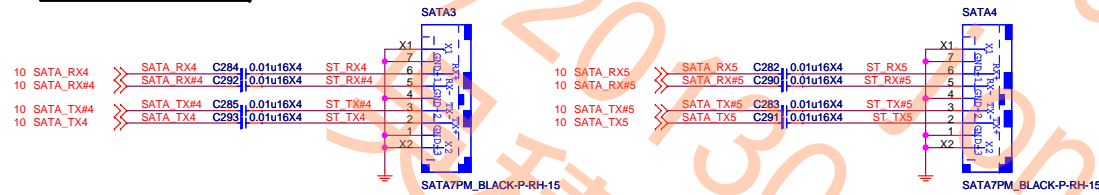
MICRO-STAR INT'L CO.,LTD			
MS-7817			
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Custom	LAN RTL8111G/8106E	12	
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## SATA 6G PORT 0,1



## SATA 3G PORT 4,5



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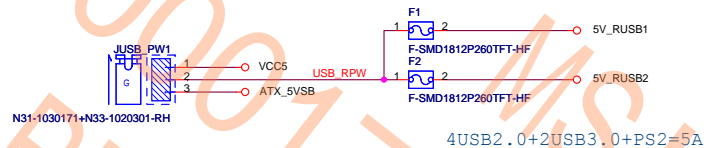
**MS-7817**

Size	Document Description	Rev
Custom	SATA Connector	12
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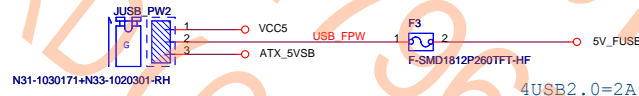
## Type C: jumper +Fuse

PCH/FCH side: OC# pull high to +3VSB

Near Rear ==>



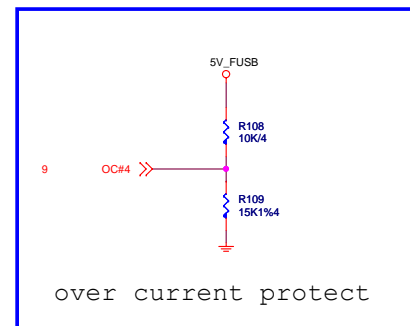
Near Front ==>



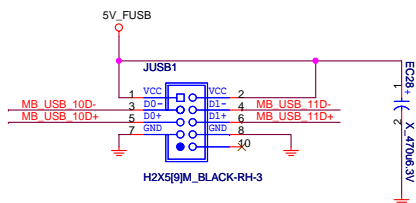
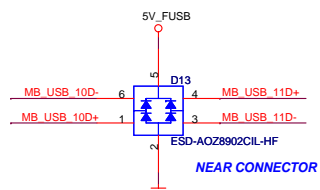
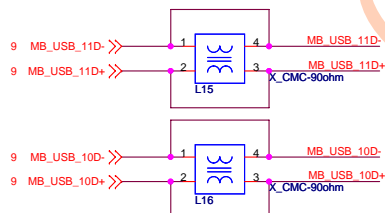
D08-2000300-P16 (Itrip=3.5A; 0.003ohm) support 6 USB ports (3A)  
D08-0300700-P16 (Itrip=2.6A; 0.015ohm) support 4 USB ports (2A)  
D08-0100110-P16 (Itrip=1.1A; 0.04ohm) support 2 usb 2.0 ports (1A)

### Default VCC5 (PIN1-2)

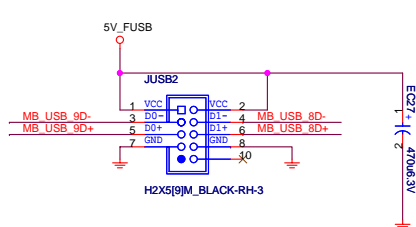
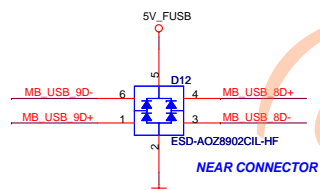
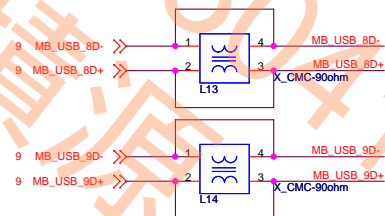
JUSB_FW	BIOS Menu	Wake up support
1-2	EUP Enable	Not support
	EUP Disable	
2-3	EUP Enable	Not support
	EUP Disable	support



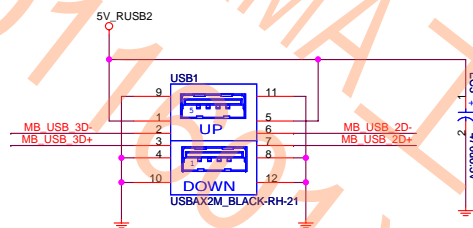
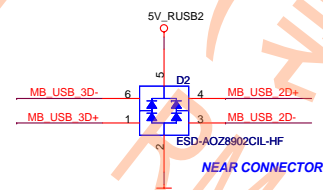
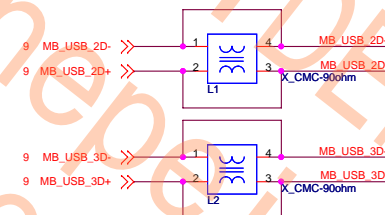
### FRONT USB PORT 8,9



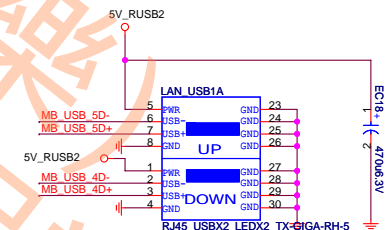
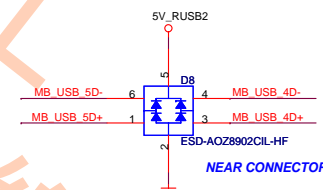
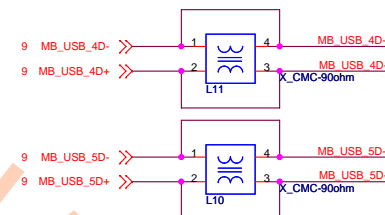
### FRONT USB PORT 10,11



### FRONT USB PORT 10,11



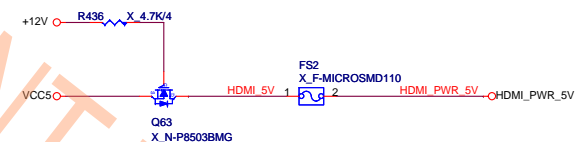
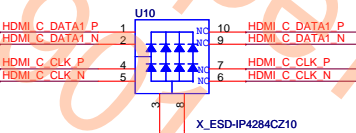
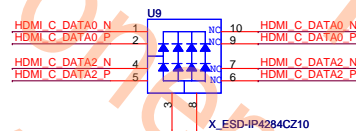
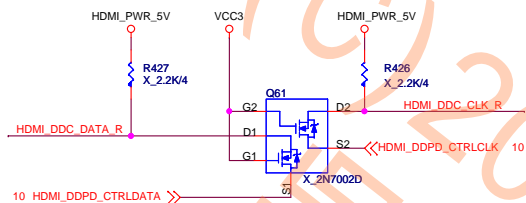
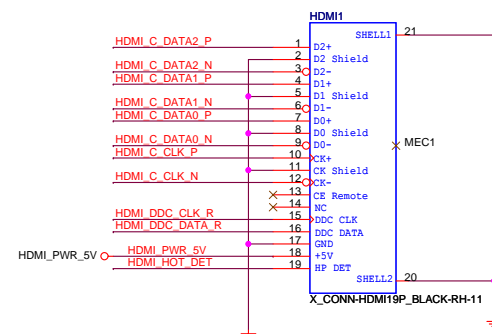
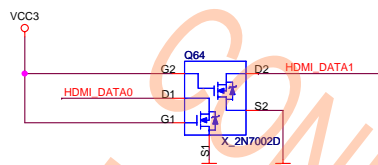
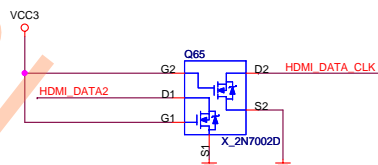
### FRONT USB PORT 10,11



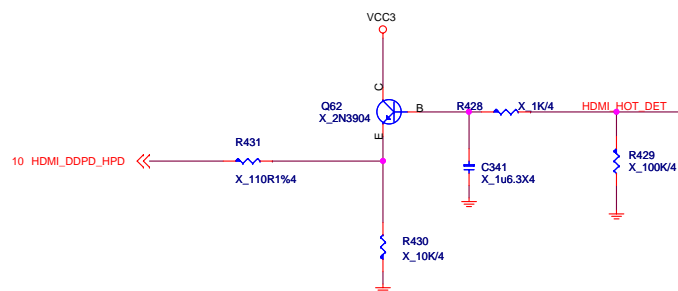
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

3	HDMI_DDPD_CLK_P	C333	X 0.1u10X4	HDMI C CLK P	R419	X 470R/4	HDMI DATA_CLK
3	HDMI_DDPD_CLK_N	C338	X 0.1u10X4	HDMI C CLK N	R418	X 470R/4	
3	HDMI_DDPD_TX2_P	C340	X 0.1u10X4	HDMI C DATA2 P	R422	X 470R/4	HDMI DATA2
3	HDMI_DDPD_TX2_N	C337	X 0.1u10X4	HDMI C DATA2 N	R420	X 470R/4	
3	HDMI_DDPD_TX1_P	C339	X 0.1u10X4	HDMI C DATA1 P	R425	X 470R/4	HDMI DATA1
3	HDMI_DDPD_TX1_N	C336	X 0.1u10X4	HDMI C DATA1 N	R423	X 470R/4	
3	HDMI_DDPD_TX0_P	C335	X 0.1u10X4	HDMI C DATA0 P	R421	X 470R/4	HDMI DATA0
3	HDMI_DDPD_TX0_N	C334	X 0.1u10X4	HDMI C DATA0 N	R424	X 470R/4	



HPD



For EMI

HDMI C CLK N	R432	X_180R/1%4
HDMI C CLK P	R433	X_180R/1%4
HDMI C DATA0 N	R434	X_180R/1%4
HDMI C DATA0 P	R435	X_180R/1%4
HDMI C DATA1 N	R436	X_180R/1%4
HDMI C DATA1 P	R437	X_180R/1%4
HDMI C DATA2 N	R438	X_180R/1%4
HDMI C DATA2 P	R439	X_180R/1%4

EMI

HDMI DDC CLK R	C342	X 0.1u10X4
HDMI DDC DATA R	C344	X 0.1u10X4
HDMI HOT_DET	C343	X 0.1u10X4



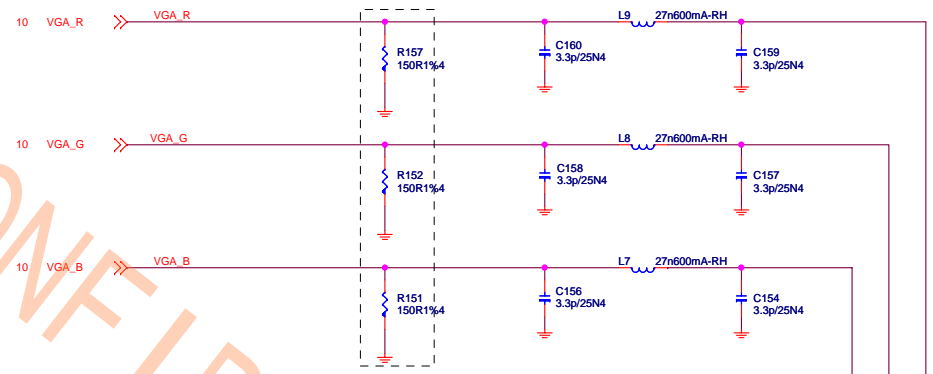
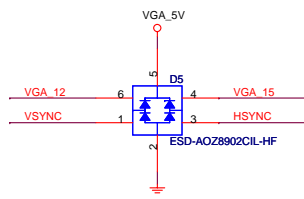
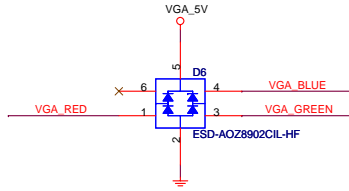
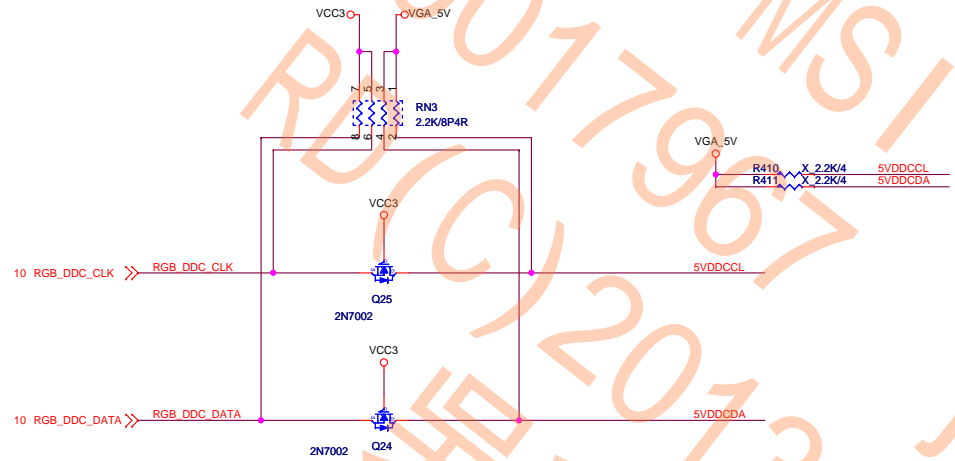
MICRO-STAR INT'L CO.,LTD

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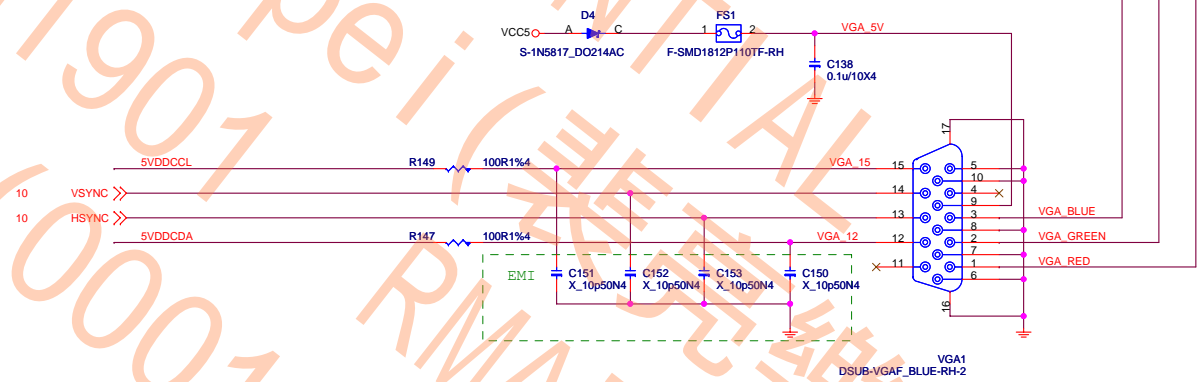
Size	Custom	Document Description	HDMI Connector	Rev	12
Date:	Tuesday, March 19, 2013	Sheet	22	of	36

D-Sub

Level shift

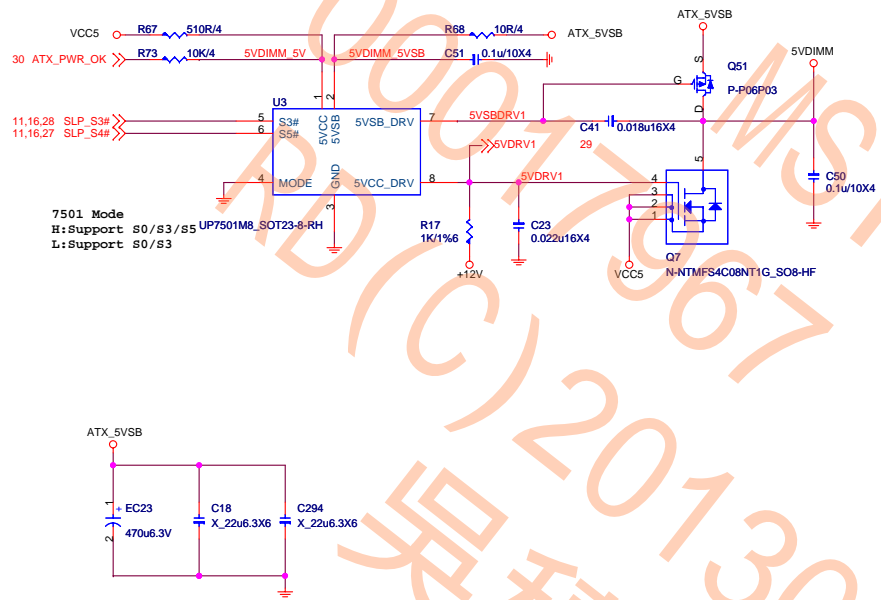


PLACE CLOSE TO VGA CONNECTOR,  
WITHIN 750 MIL OF PIN

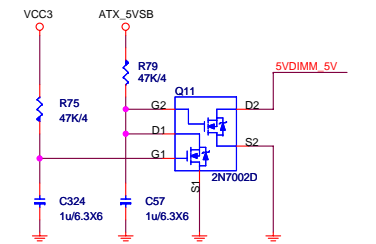




## 5VDIMM FOR DDR



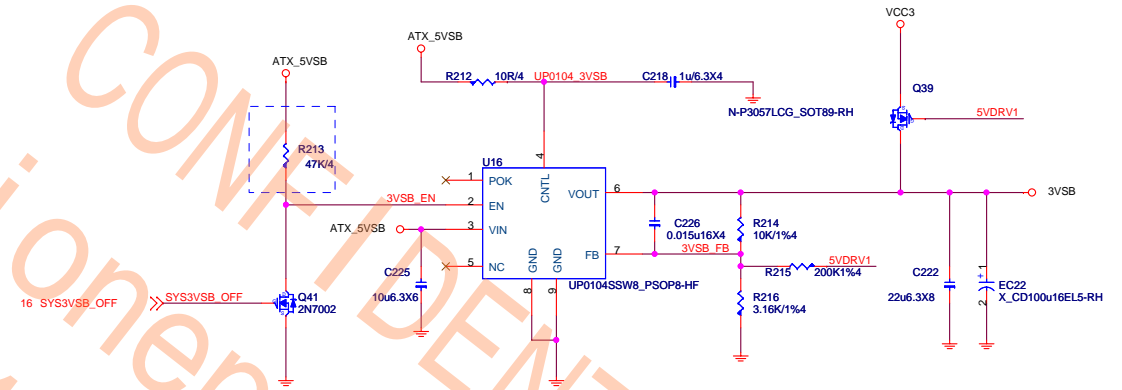
For power 700W solution (only for uP7501+uP7506 for 3VSB solution)  
The power supply VCC3 delay 12ms after VCC5 assert.  
The chip U7501 5VDRV1 work when the VCC5 ready  
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but  
VCC3 not ready and let the 3VSB sequence fail.



### Patch coolermaster 700w power sequence

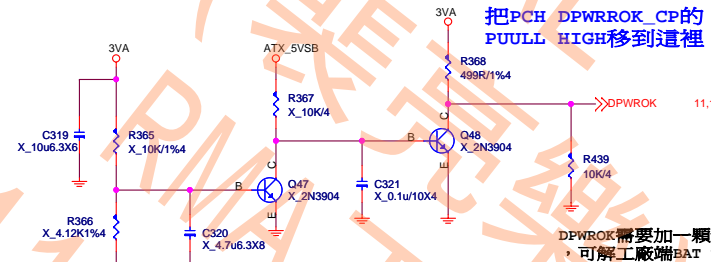
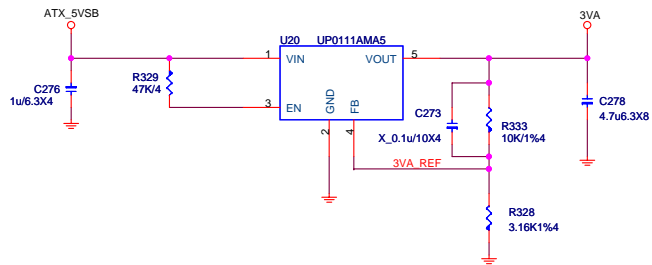
### 3VSB

3VSB supply to PCH and other device.  
Turn off when Deep S3/S5 by 5VSB off.



3VA

20mA



DPWROK需要加一顆pull down 10k電阻  
，可解工廠端BAT 電流過大問題

$$3.389V \text{分壓} = 0.813V$$
$$2.71V \text{ 分壓 } = 0.65V$$

FOR DPWROK跟3VA的POWER  
DOWN的時序(S5-->G3)

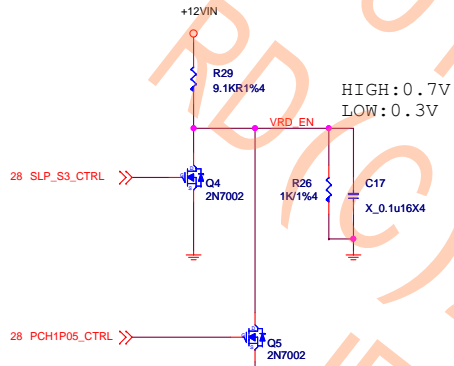


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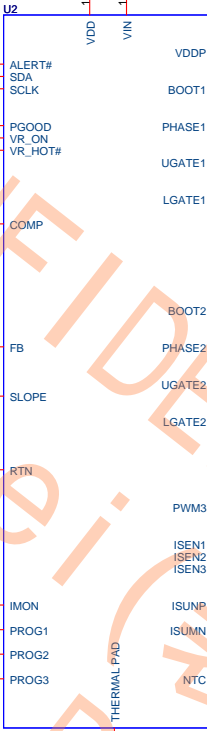
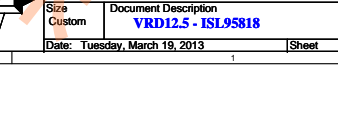
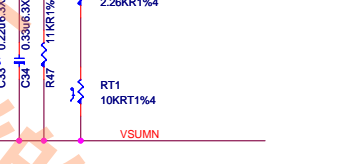
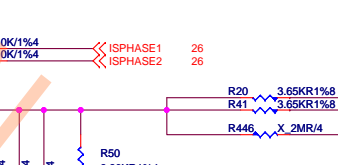
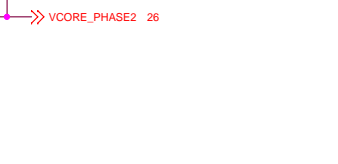
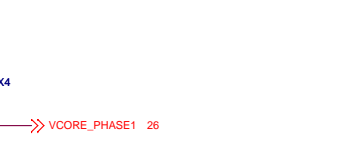
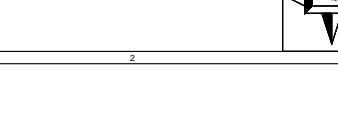
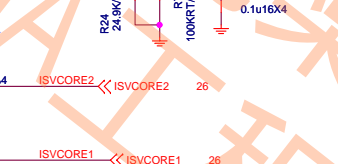
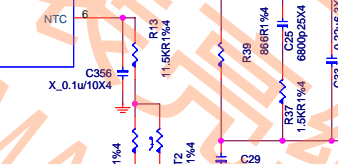
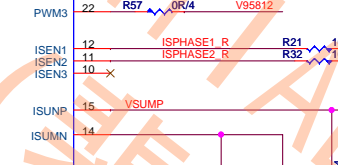
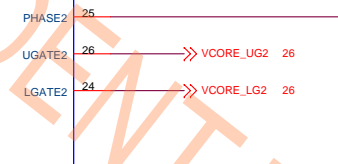
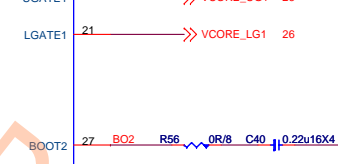
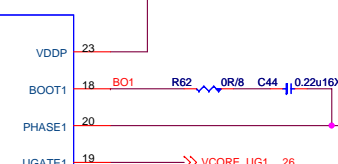
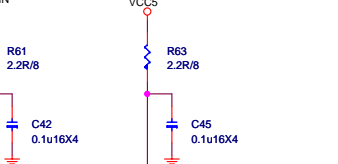
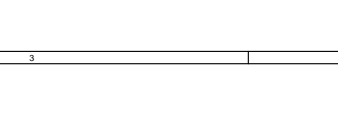
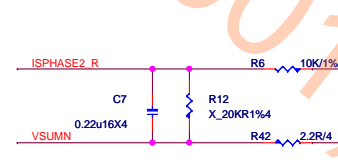
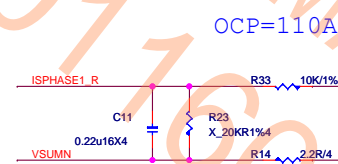
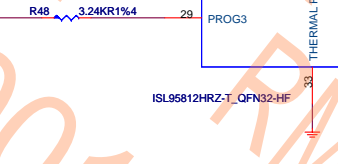
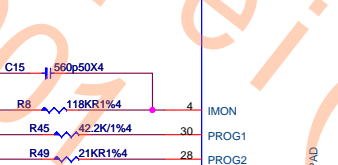
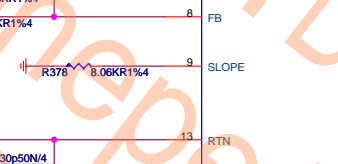
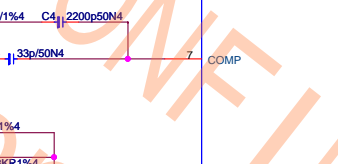
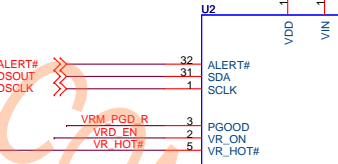
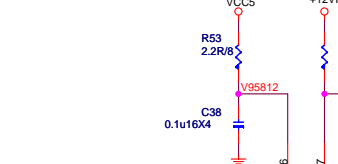
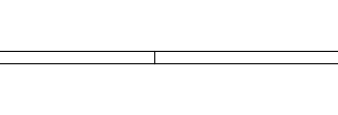
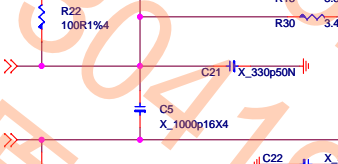
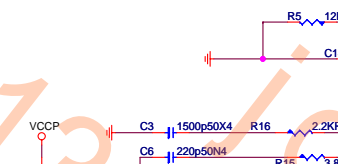
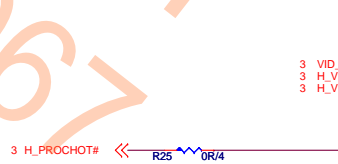
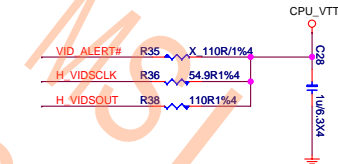
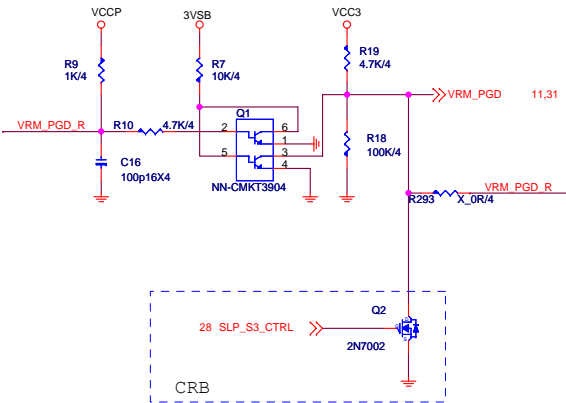
VCORE power on by s3 and 12v



CRB

HIGH:by PCH\_1P05V  
LOW:by S3

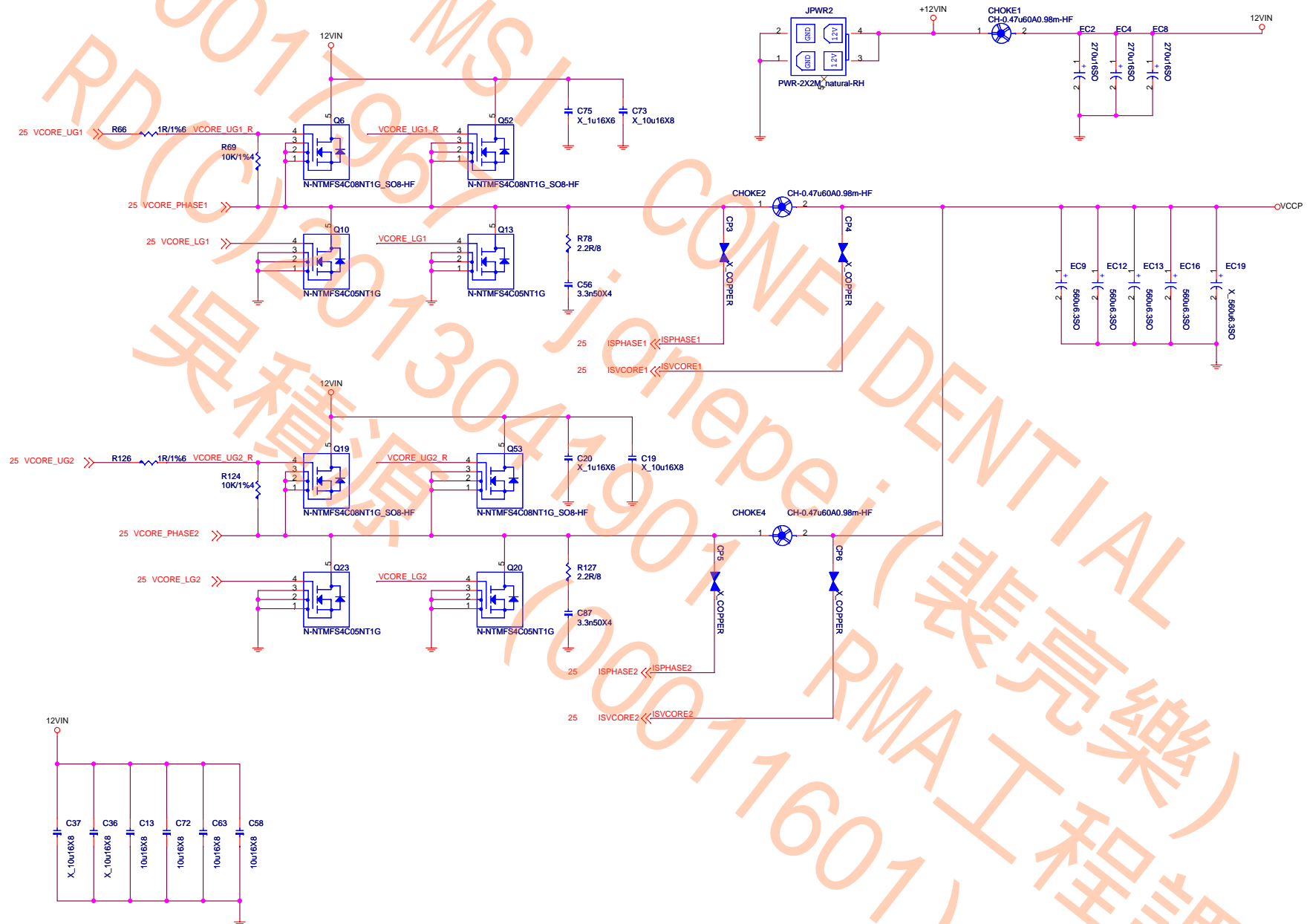
#### VRMPWRGD LEVEL SHIFT



OCP=110A

# VCCP POWER

VCORE ICC MAX70A ICCTDC:47A 65W  
LL:2.5m ohm



OCP: 28A

#### 4.2A FOR CPU

**6A FOR 2DIMM**

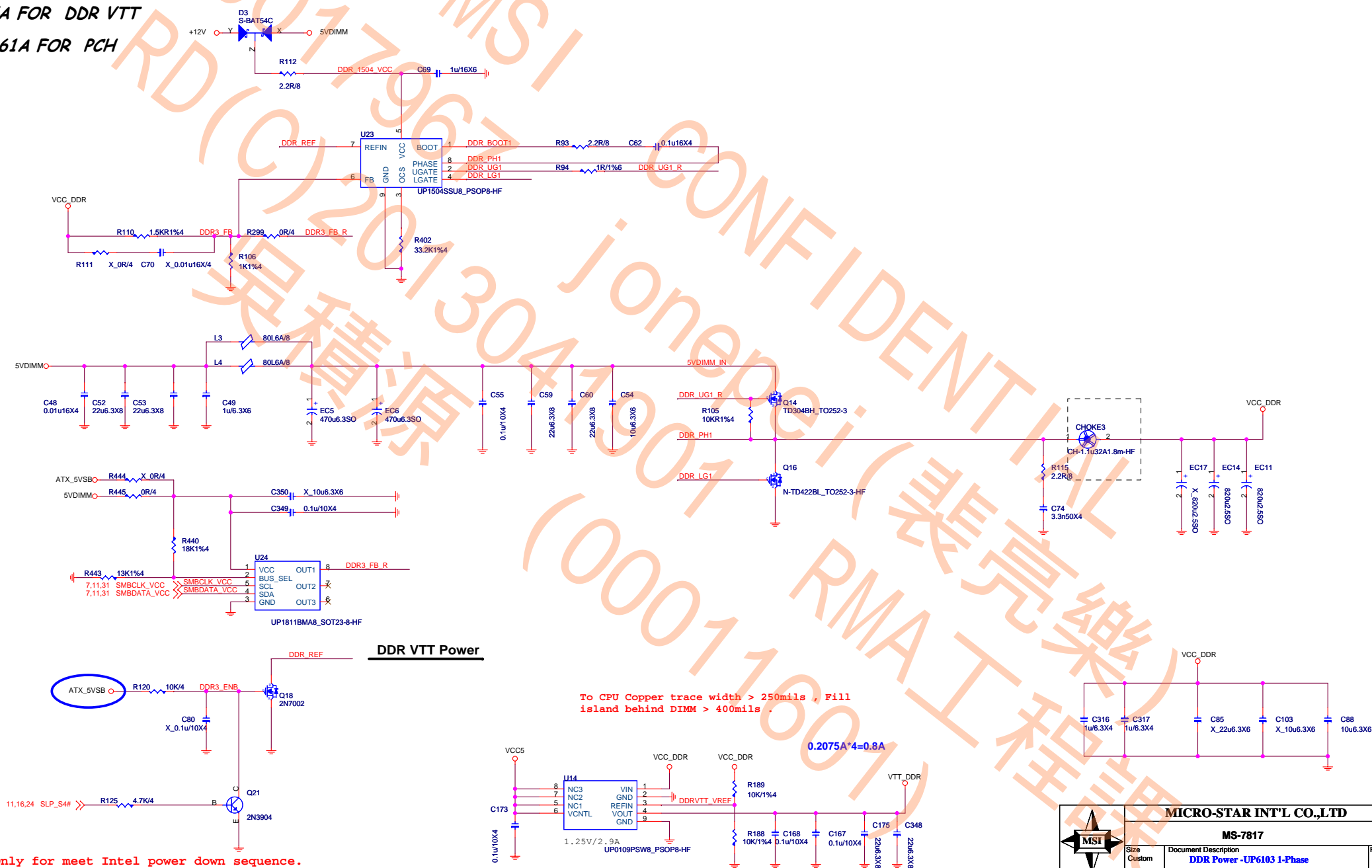
**0.5A FOR DDR VTT**

**7.661A FOR PCH**

***OCP:16.447\*1.5=24.6705A***

$$OCPXR_{dson}(Low\ side)=(40\mu A * R_{ocs}(R122))-0.4V$$

***Rocs(R122)=13.75K***



### DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

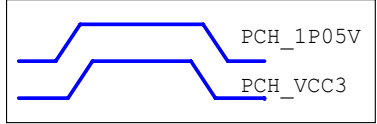
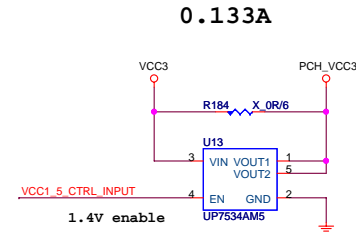
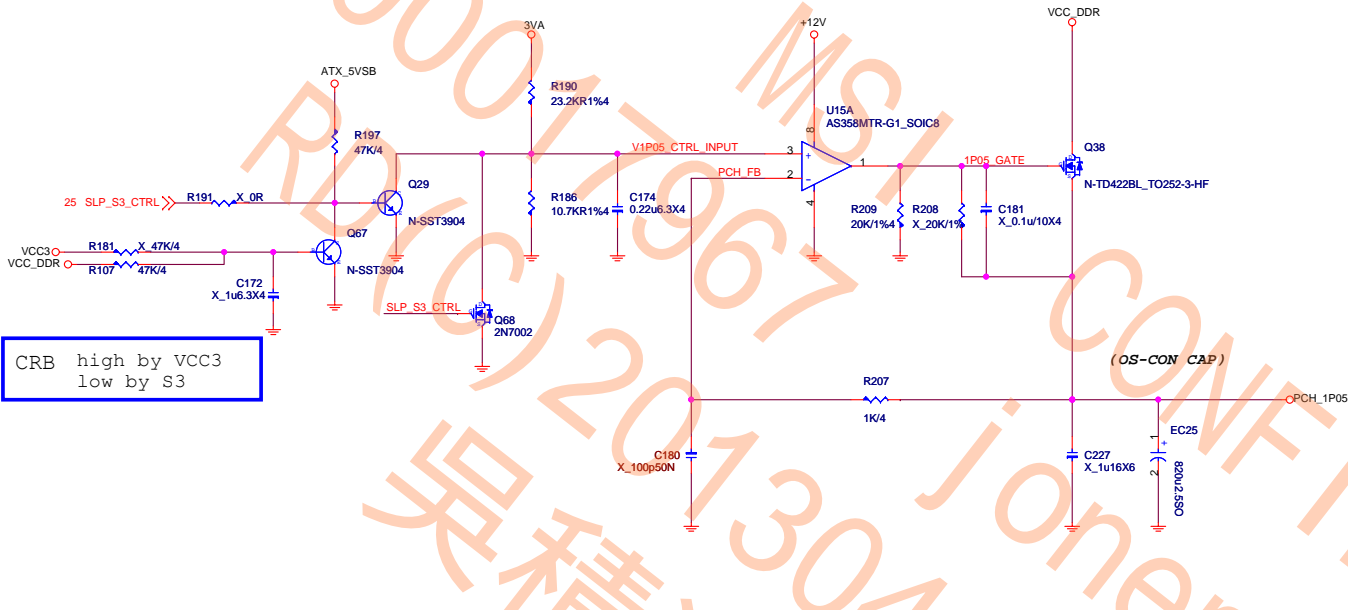
$$0.2075A \cdot 4 = 0.8A$$

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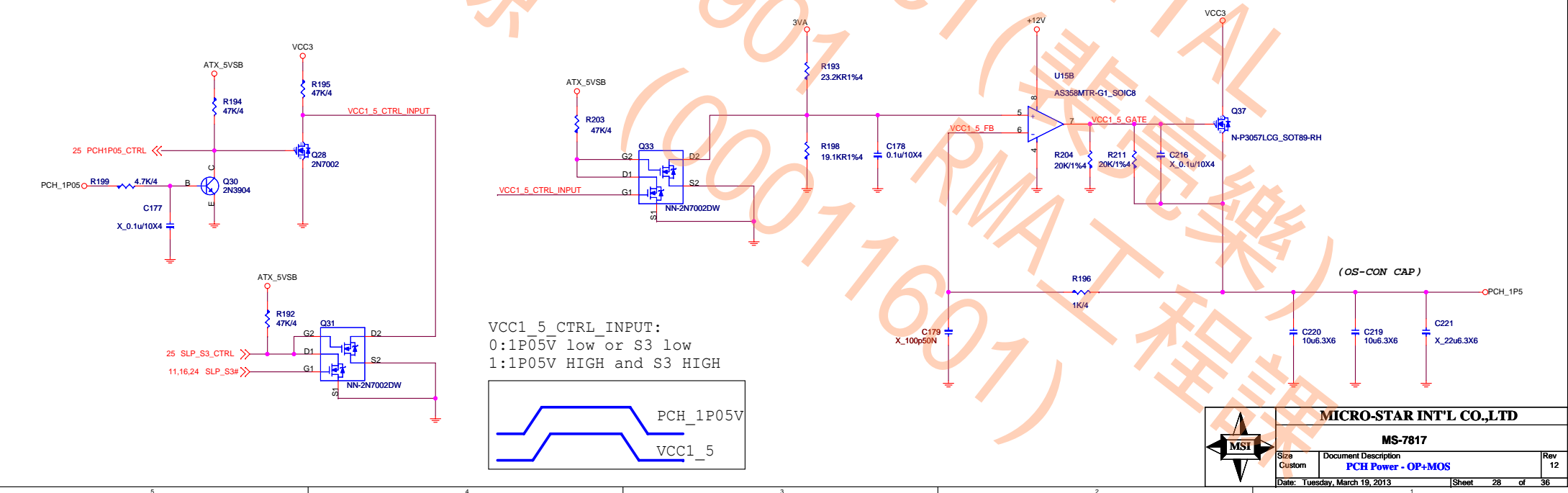
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Size Custom	Document Description <b>DDR Power -UP6103 1-Phase</b>	Rev 12
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PCH Power:1.05V 5.747A

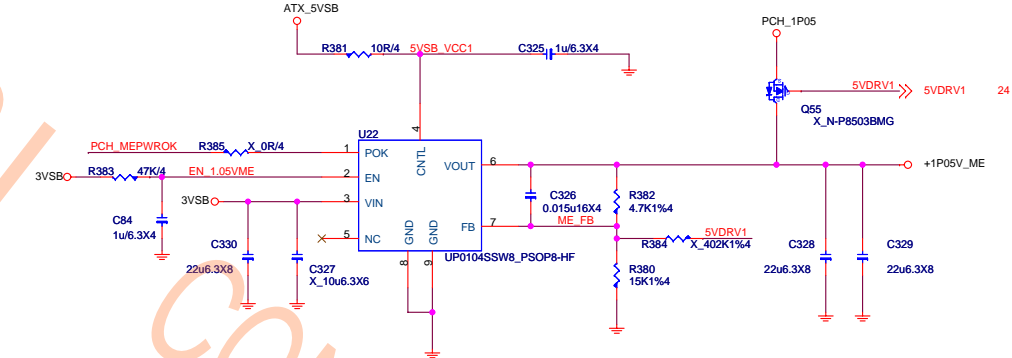
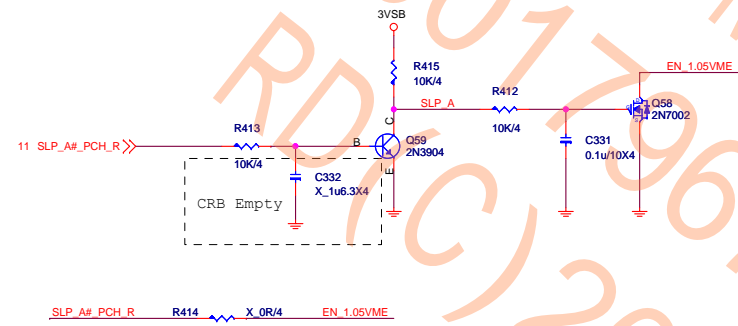


PCH Power:1.5V 0.183A

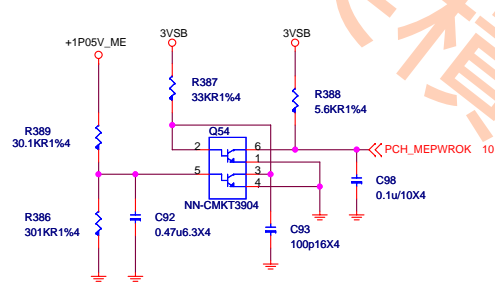


SLP\_A

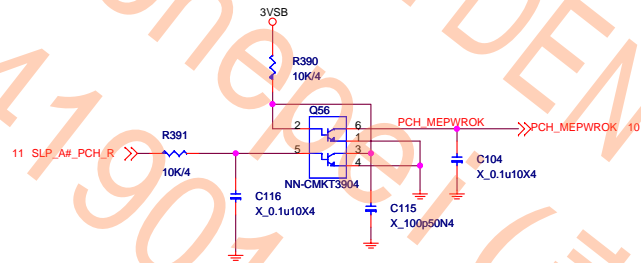
ME Power Control



PCH\_MEPWROK



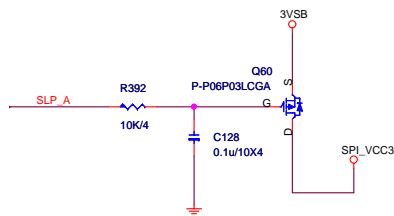
VccASW active to APWROK high 1ms



APWROK falling to VccASW falling 40ns

+3.3V\_ME

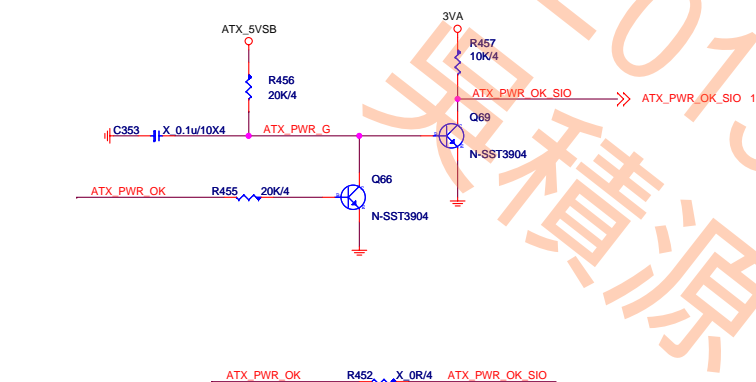
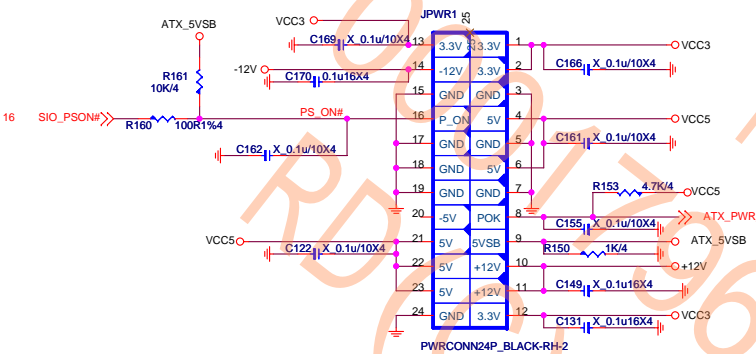
+3.3V\_ME



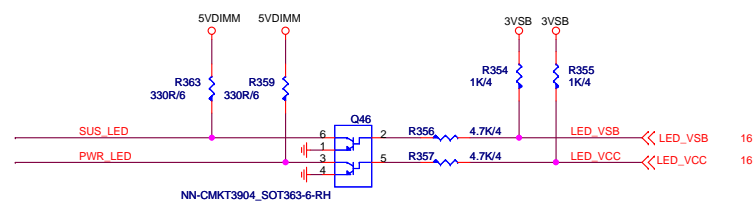
For INTEL ME  
VCC3 - R393 X 0R/6 - OSPI\_VCC3  
H81 STUFF



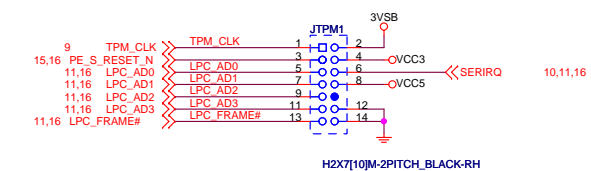
## ATX POWER CONNECTOR



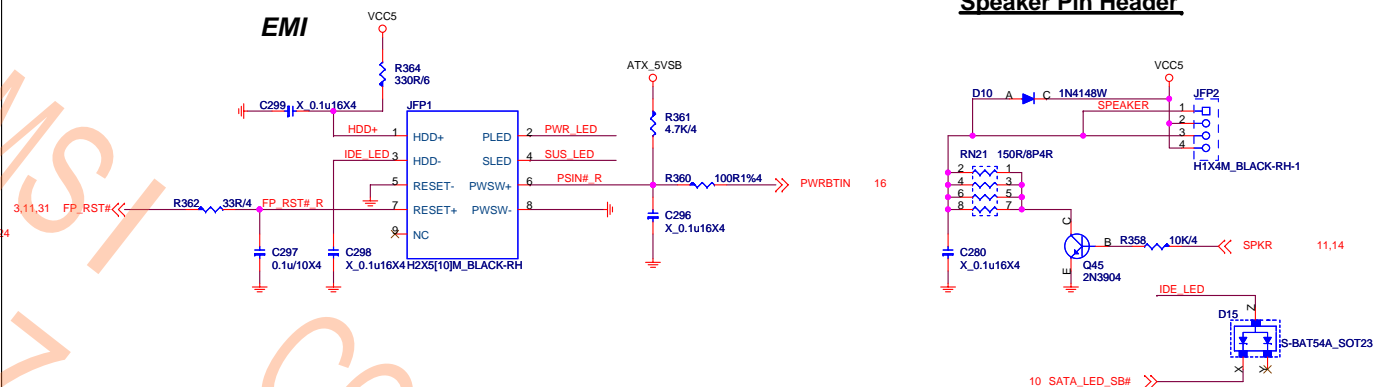
**LED ( for NV5533)**



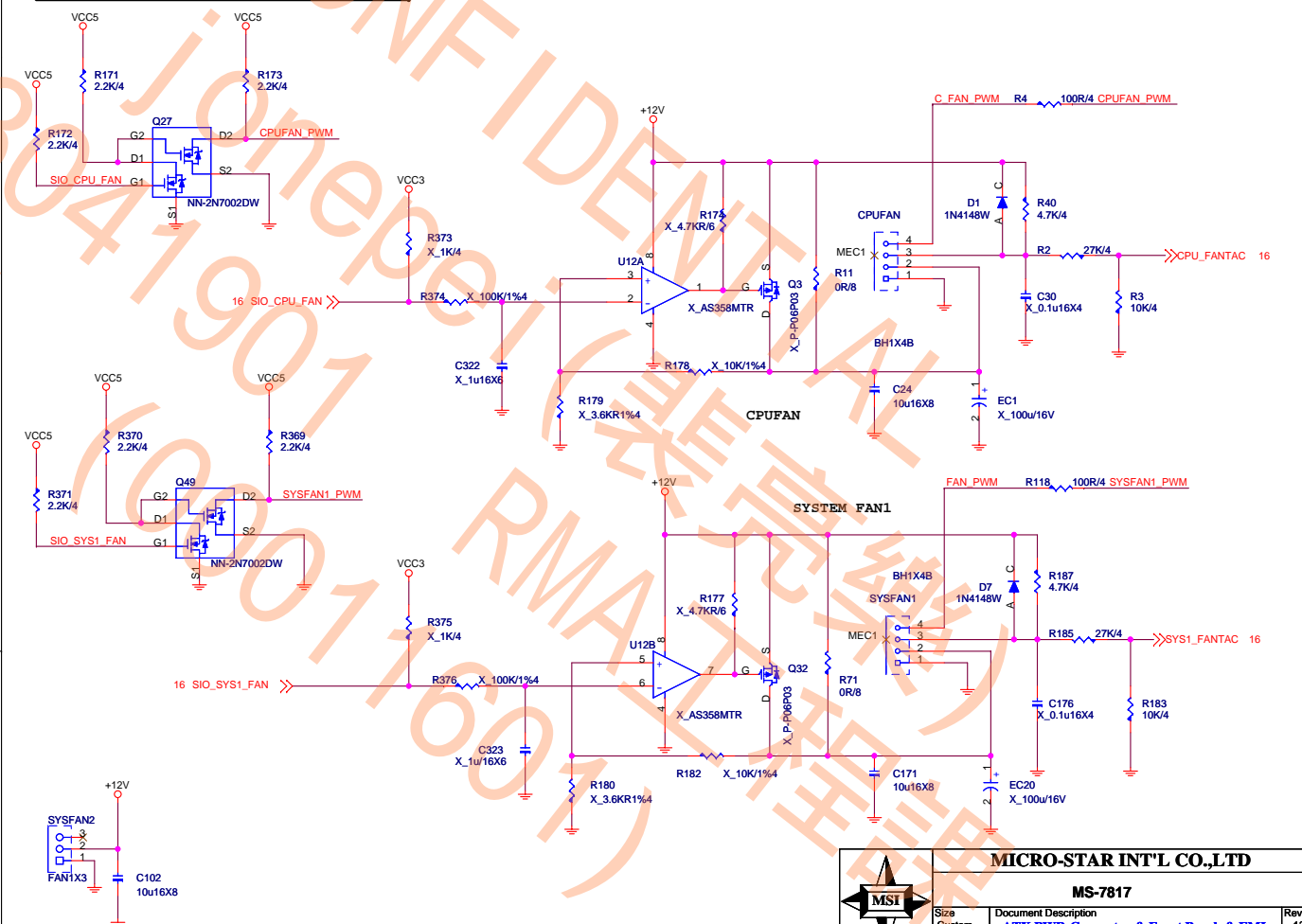
*TPM/JLPC*



FRONT PANNEL



## FAN-COUNTROL CIRCUIT

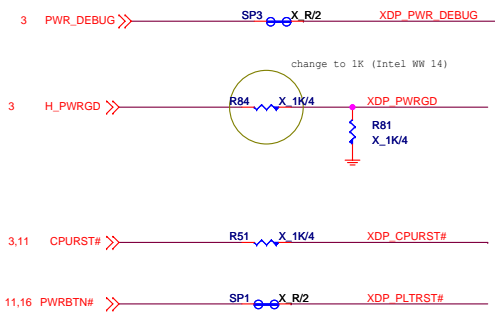
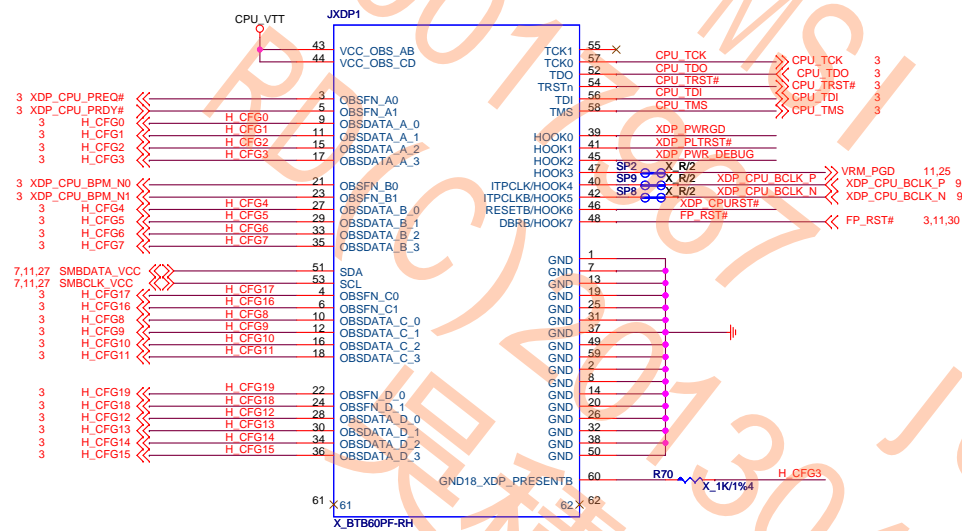


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## Reserve debug port 5020



PLACE NEAR XDP CONNECTOR

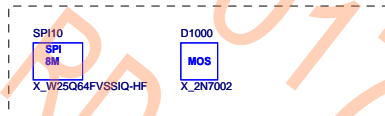


MICRO-STAR INT'L CO.,LTD

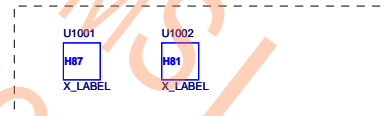
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Custom	XDP CPU & PCH	12
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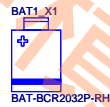
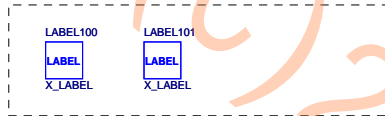
# SPI OPT.



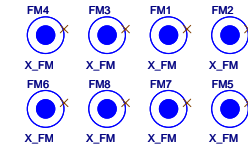
# CHIPSET OPT.



# LABEL OPT.



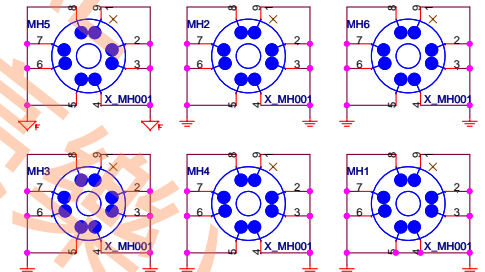
# Optical Fiducial Marks-120



# Simulation



# Mounting Holes



# PCH XDP PWRGD/RESET

